

## Features

- 16-/32-bit Data and Address Register
- 16-Mbyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped Input/Output
- 14 Addressing Modes
- Three Available Versions: 8 MHz/10 MHz and 12.5 MHz
- Military Temperature Range: -55/+125°C
- Power Supply: 5V<sub>DC</sub> ± 10%

## Description

The TS68C000 reduced power consumption device dissipates an order of magnitude less power than the HMOS TS68000. The TS68C000 is an implementation of the TS68000 16/32 microprocessor architecture. The TS68C000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data-buses. It is completely code-compatible with the HMOS TS68000, TS68008 8-bit data bus implementation of the TS68000 and the TS68020 32-bit implementation of the architecture. Any user-mode programs written using the TS68C000 instruction set will run unchanged on the TS68000, TS68008 and TS68020. This is possible because the user programming model is identical for all processors and the instruction sets are proper sub-sets of the complete architecture.

## Screening/Quality

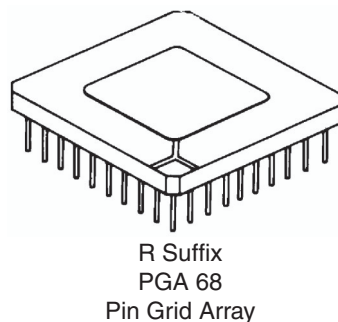
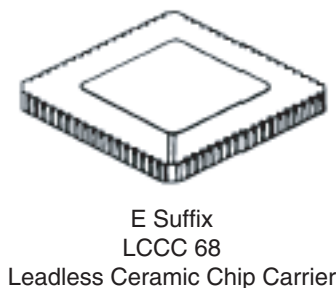
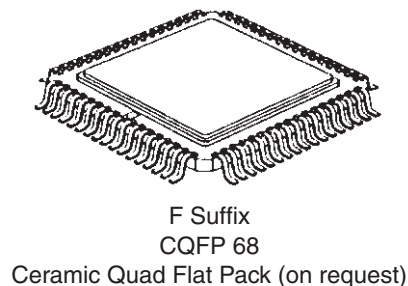
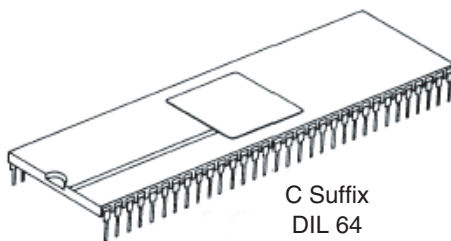
This product is manufactured in full compliance with:

- MIL-STD-883 class B
- DESC drawing 5962-89462
- Atmel standards



## Low Power HCMOS 16-/32-bit Hi-Rel Microprocessor

## TS68C000



Rev. 2170A-HIREL-09/05



## 1. General Description

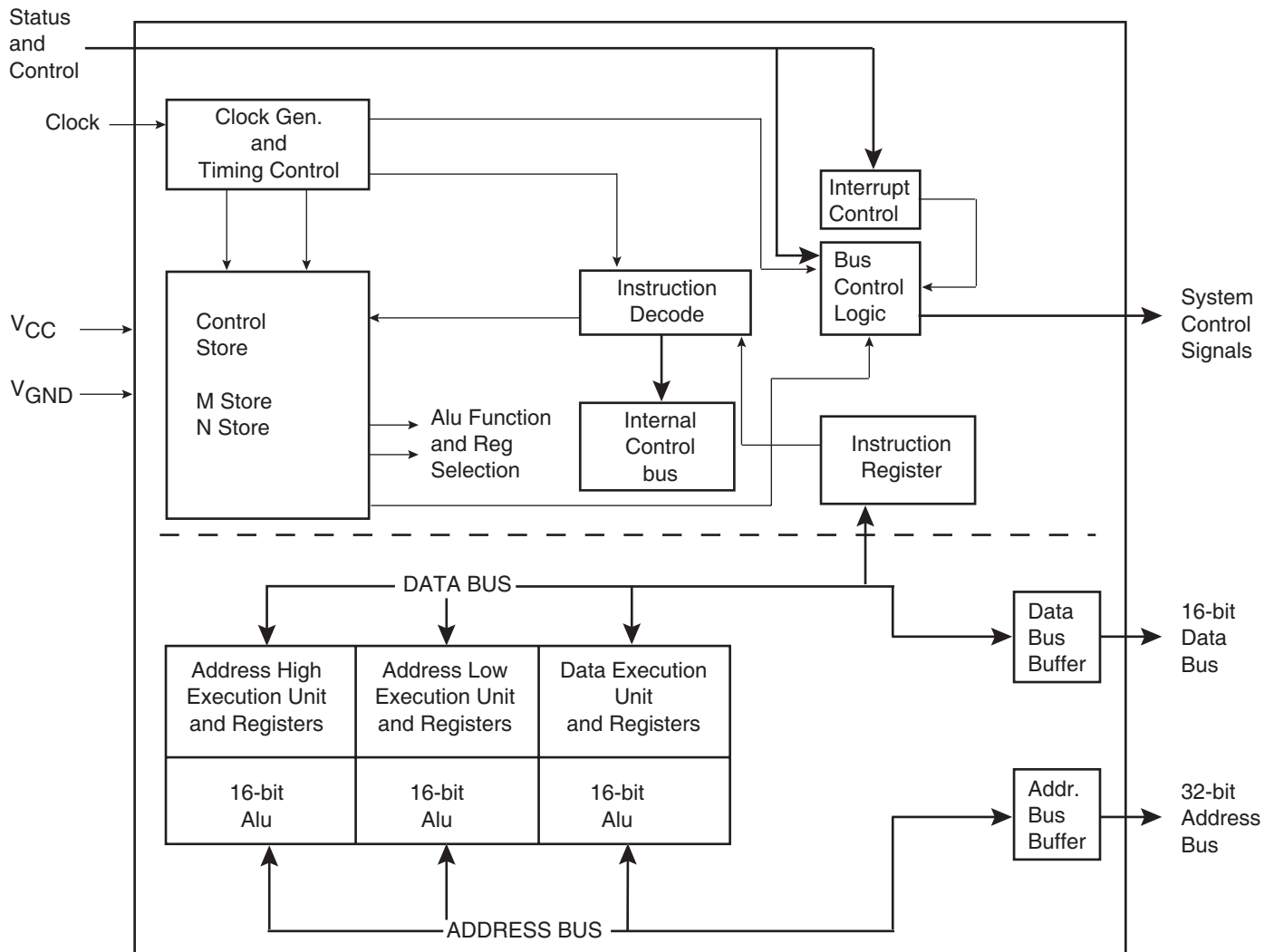
### 1.1 Introduction

This detail specification contains both a summary of the TS68C000 as well as detailed set of parametrics. The purpose is twofold to provide an instruction to the TS68C000 and support for the sophisticated user. For detail information on the TS68C000, refer to "68000 16-bit microprocessor user's manual".

### 1.2 Detailed Block Diagram

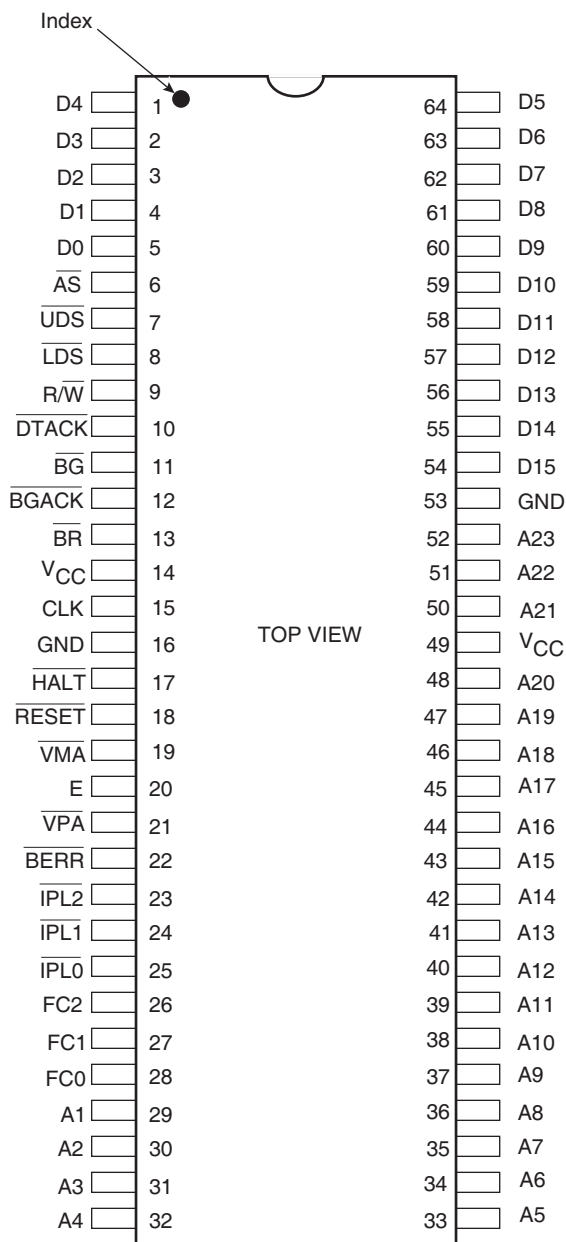
The functional block diagram is given in [Figure 1-1](#) below.

**Figure 1-1.** Block Diagram

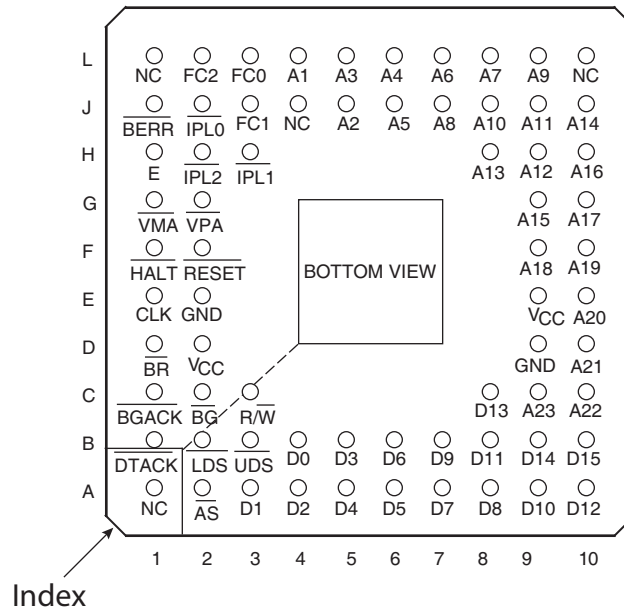


## 1.3 Pin Assignments

Figure 1-2. 64-lead Dual-in-Line Package



**Figure 1-3.** 68-terminal Pin Grid Array



**Figure 1-4.** 68-lead Quad Pack

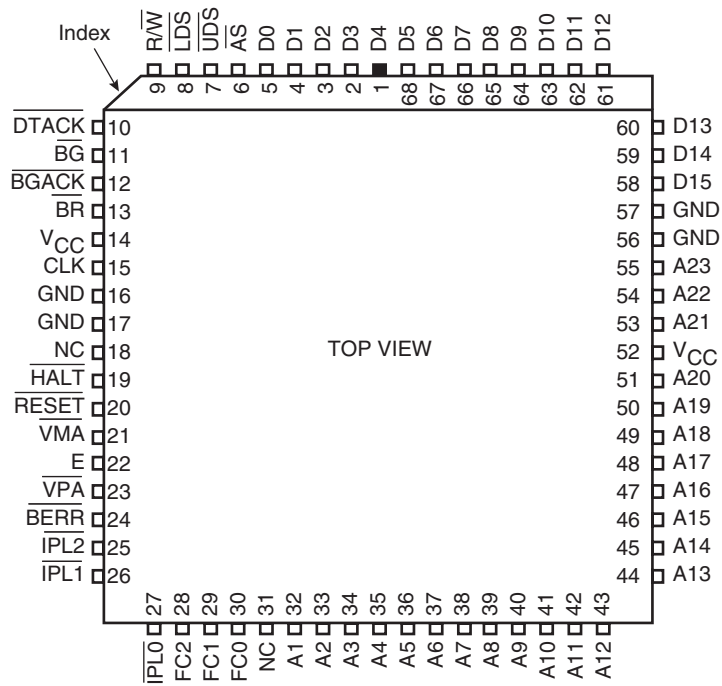
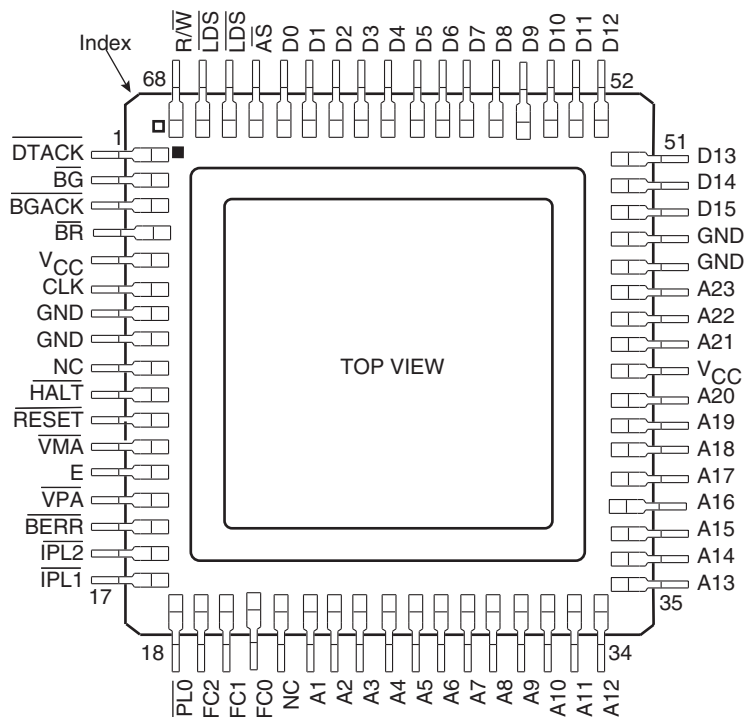


Figure 1-5. 68-ceramic Quad Flat Pack



## 1.4 Terminal Designations

The function, category and relevant symbol of each terminal of the device are given in the following table.

Table 1-1. Terminal Designations

| Symbol                                 | Function                   | Category  |
|----------------------------------------|----------------------------|-----------|
| $V_{CC}$                               | Power supply (2 terminals) | Supply    |
| $V_{SS}^{(1)}$                         | Power supply (2 terminals) | Terminals |
| FC0 to FC2                             | Processor status           | Outputs   |
| $\overline{IPL0}$ to $\overline{IPL2}$ | Interrupt control          | Inputs    |
| A1 to A23                              | Address bus                | Outputs   |
| AS                                     | Asynchronous bus control   | Outputs   |
| $R/\overline{W}$                       |                            |           |
| $\overline{UDS}$                       |                            |           |
| $\overline{LDS}$                       |                            |           |
| $\overline{DTACK}$                     |                            | Input     |
| $\overline{BR}$                        | Bus arbitration control    | Inputs    |
| $\overline{BGACK}$                     |                            |           |
| $\overline{BG}$                        |                            | Output    |

**Table 1-1.** Terminal Designations (Continued)

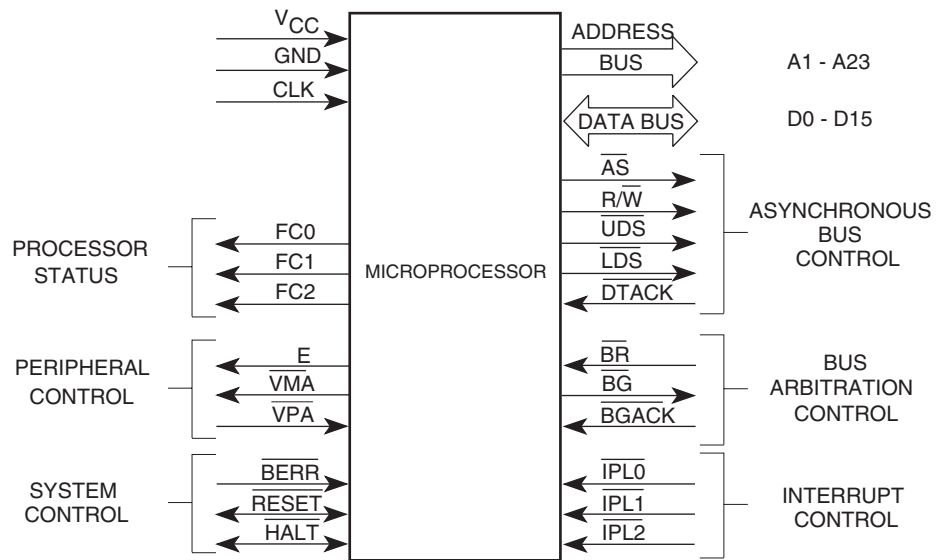
| Symbol                    | Function                | Category     |
|---------------------------|-------------------------|--------------|
| $\overline{\text{BERR}}$  | System control          | Input        |
| $\overline{\text{RESET}}$ |                         | Input/Output |
| $\overline{\text{HALT}}$  |                         |              |
| $\overline{\text{VPA}}$   | 6800 peripheral control | Input        |
| $\overline{\text{VMA}}$   |                         | Output       |
| E                         |                         | Output       |
| CLK                       | Clock                   | Input        |
| D0 to D15                 | Data bus                | Input/Output |

Note: 1.  $V_{SS}$  is the reference terminal for the voltages

## 1.5 Signal Description

The input and output signals are illustrated functionally in [Figure 1-6](#) and are described in the following paragraphs.

**Figure 1-6.** Input and Output Signals



**Table 1-2.** Data Strobe Control of Data Bus

| $\overline{\text{UDS}}$ | $\overline{\text{LDS}}$ | R/W  | D8-D15               | D0-D7                |
|-------------------------|-------------------------|------|----------------------|----------------------|
| High                    | High                    |      | No valid data        | No valid data        |
| Low                     | Low                     | High | Valid data bits 8-15 | Valid data bits 0-7  |
| High                    | Low                     | High | No valid data        | Valid data bits 0-7  |
| Low                     | High                    | High | Valid data bits 8-15 | No valid data        |
| Low                     | Low                     | Low  | Valid data bits 8-15 | Valid data bits 0-7  |
| High                    | Low                     | Low  | Valid data bits 0-7  | Valid data bits 0-7  |
| Low                     | High                    | High | Valid data bits 8-15 | Valid data bits 8-15 |

### 1.5.0.1 *Address Bus (A1 through A23)*

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

### 1.5.0.2 *Data Bus (D0 Through D15)*

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-07.

### 1.5.0.3 *Asynchronous Bus Control*

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

#### ADDRESS STROBE ( $\overline{AS}$ )

This signal indicates that there is a valid address on the address bus.

#### READ/WRITE ( $R/\overline{W}$ )

This signal defines the data bus transfer as a read or write cycle. The  $R/\overline{W}$  signal also works in conjunction with the data strobes as explained in the following paragraph.

#### UPPER AND LOWER DATA STROBE ( $\overline{UDS}$ , $\overline{LDS}$ )

These signals control the flow of data on the data bus, as shown in [Table 1-2](#). When the  $R/\overline{W}$  line is high, the processor will read from the data bus as indicated. When the  $R/\overline{W}$  line is low, the processor will write to the data bus as shown.

#### DATA TRANSFER ACKNOWLEDGE ( $\overline{DTACK}$ )

This input indicates that the data transfer is completed. When the processor recognizes  $\overline{DTACK}$  during a read cycle, data is latched and the bus cycle terminated. When  $\overline{DTACK}$  is recognized during a write cycle, the bus cycle is terminated.

### 1.5.0.4 *Bus Arbitration Control*

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

#### BUS REQUEST ( $\overline{BR}$ )

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

#### BUS GRANT ( $\overline{BG}$ )

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

#### BUS GRANT ACKNOWLEDGE ( $\overline{BGACK}$ )

This input indicates that some other device has become the bus master.

This signal should not be asserted until the following four conditions are met:

1. a bus grant has been received,
2. address strobe is inactive which indicates that the microprocessor is not using the bus,
3. data transfer acknowledge is inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

#### 1.5.0.5 *Interrupt Control ( $\overline{IPL0}$ , $\overline{IPL1}$ , $\overline{IPL2}$ )*

These Input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in  $\overline{IPL0}$  and the most significant bit is contained in  $\overline{IPL2}$ . These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

#### 1.5.0.6 *System Control*

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

##### BUS ERROR ( $\overline{BERR}$ )

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

##### RESET ( $\overline{RESET}$ )

This bidirectional signal line acts to reset (start a system initialization sequence) to processor in response to an external reset signal. An internally generated reset (result of a  $\overline{RESET}$  instruction) causes all external devices to be reset and the internal of the processor is not affected. A total system reset (processor and external devices) is the result of external  $\overline{HALT}$  and  $\overline{RESET}$  signals applied at the same time.

##### HALT ( $\overline{HALT}$ )

When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state.

When the processor has stopped executing Instructions, such as in a double bus fault condition, the  $\overline{HALT}$  line is driven by the processor to indicate to external devices that the processor has stopped.

### 1.5.0.7 EF 6800 Peripheral Control

These control signals are used to allow the interfacing of synchronous EF 6800 peripheral devices with the asynchronous TS68C000. These signals are explained in the following paragraphs.

#### ENABLE (E)

This signal is the standard enable signal common to all EF 6800 type peripheral devices. The period for this output is ten TS68C000 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running crack and runs regardless of the state of the bus on the MPU.

#### VALID PERIPHERAL ADDRESS ( $\overline{\text{VPA}}$ )

This input indicates that the device or region addressed is an TS68000 Family device and that data transfer should be synchronized with the enable (E) signal. This Input also indicates that the processor should use automatic vectoring for an interrupt during an IACK cycle.

#### VALID MEMORY ADDRESS ( $\overline{\text{VMA}}$ )

This output is used to indicate to TS68000 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ( $\overline{\text{VPA}}$ ) input which indicates that the peripheral is an TS68000 Family device.

### 1.5.0.8 Processor Status (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in [Table 1-3](#). The information indicated by the function code outputs is valid whenever address strobe ( $\overline{\text{AS}}$ ) is active.

**Table 1-3.** Processor Status Table

| Function Code Output |      |      | Cycle Time            |
|----------------------|------|------|-----------------------|
| FC2                  | FC1  | FC0  |                       |
| Low                  | Low  | Low  | (Undefined, reserved) |
| Low                  | Low  | High | User data             |
| Low                  | High | Low  | User program          |
| Low                  | High | High | (Undefined, reserved) |
| High                 | Low  | Low  | (Undefined, reserved) |
| High                 | Low  | High | Supervisor data       |
| High                 | High | Low  | Supervisor program    |
| High                 | High | High | Interrupt acknowledge |

### 1.5.0.9 Clock (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times. The clock is a constant frequency square wave with no stretching or shaping techniques required.

## 2. Detailed Specifications

### 2.1 Scope

This drawing describes the specific requirements for the microprocessor TS68C000, 8 MHz, 10 MHz and 12.5 MHz, in compliance with MIL-STD-883 class B.

### 2.2 Applicable Documents

#### 2.2.1 MIL-STD-883

1. MIL-STD-883: Test Methods and Procedures For Electronics
2. MIL-PRF-38535 Appendix A: General Specifications for Microcircuits

### 2.3 Requirements

#### 2.3.1 General

The microcircuits are in accordance with the applicable document and as specified herein.

### 2.4 Design and Construction

#### 2.4.1 Terminal Connections

Depending on the package, the terminal connections shall be as shown in [Figure 1-2](#), [Figure 1-3](#), [Figure 1-4](#) and [Figure 1-5](#).

#### 2.4.2 Lead Material and Finish

Lead material and finish shall be any option of MIL-PRF-38535 Appendix A-3-5-6 "Package Element Material and Finish".

#### 2.4.3 Package

The macrocircuits are packaged in hermetically sealed ceramic package which is conform to case outlines of MIL-PRF-38535 Appendix A-3-5-1.

- PGA68 64 LEAD DIP
- 64 DILSQ. LCC 68 PINS
- 68 LCCC68 TERMINALS JCC
- 68 CQFP

The precise case outlines are described on figures and into MIL-M-38510.

#### 2.4.4 Electrical Characteristics

##### 2.4.4.1 Absolute Maximum Ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. However some limiting conditions (ratings) may be taken in other parts of this specification as detail conditions for an applicable test.

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in [Table 1-1](#), "Terminal Designations" on [page 5](#) of this specification.

**Table 2-1.** Absolute Maximum Ratings

| Symbol      | Parameter             | Test Conditions            | Min  | Max  | Unit        |
|-------------|-----------------------|----------------------------|------|------|-------------|
| $V_{CC}$    | Supply voltage        |                            | -0.3 | +6.5 | V           |
| $V_I$       | Input voltage         |                            | -0.3 | +6.5 | V           |
| $V_O$       | Output voltage        |                            | NA   | NA   | V           |
| $V_{OZ}$    | Off state voltage     |                            | -0.3 | 11.0 | V           |
| $I_O$       | Output currents       |                            | NA   | NA   | mA          |
| $I_I$       | Input currents        |                            | NA   | NA   | mA          |
| $P_{DMAX}$  | Max power dissipation | $T_{CASE} = -55^{\circ}C$  |      | 0.27 | W           |
|             |                       | $T_{CASE} = +125^{\circ}C$ |      | 0.27 | W           |
| $T_{STG}$   | Storage temperature   |                            | -55  | +150 | $^{\circ}C$ |
| $T_J$       | Junction temperature  |                            |      | +150 | $^{\circ}C$ |
| $T_{LEADS}$ | Lead temperature      | Max 5 sec. Soldering       |      | +270 | $^{\circ}C$ |

#### 2.4.4.2 Recommended Condition of Use and Guaranteed Characteristics

- Guaranteed Characteristics ([Table 2-5](#) and [Table 2-8](#))

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified below.

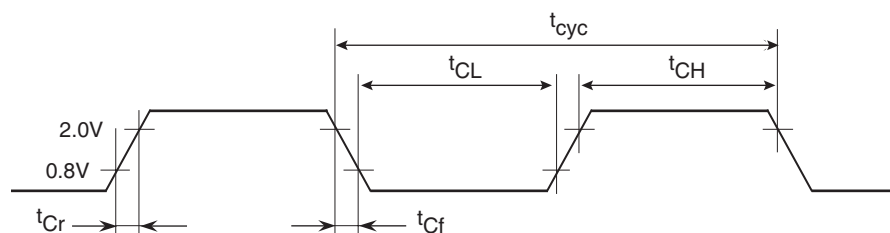
- Recommended conditions of use ([Table 2-2](#))

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test ([Table 2-9](#)).

- Additional Electrical Characteristics ([Table 2-9](#)), see "[Additional Electrical Characteristics](#)" on [page 30](#).

**Figure 2-1.** Clock Input Timing Diagram


Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8V and 2.0V.

Unless otherwise stated, all voltages are referenced to the reference terminal (see [Table 1-1](#)).

**Table 2-2.** Recommended Condition of Use

| Symbol      | Parameter                                                | Operating Range |     |          |          |
|-------------|----------------------------------------------------------|-----------------|-----|----------|----------|
|             |                                                          | Model           | Min | Max      | Unit     |
| $V_{CC}$    | Supply voltage                                           | All             | 4.5 | 5.5      | V        |
| $V_{IL}$    | Low level input voltage                                  | All             | 0   | 0.8      | V        |
| $V_{IH}$    | High level input voltage (see also "Package" on page 10) | All             | 2.0 | $V_{CC}$ | V        |
| $T_{CASE}$  | Operating temperature                                    | All             | -55 | +125     | °C       |
| $R_L$       | Value of output load resistance                          | All             | (1) |          | $\Omega$ |
| $C_L$       | Output loading capacitance                               | All             |     | (1)      | pF       |
| $t_{r(c)}$  | Clock rise time (see Figure 2-1)                         | All             |     | 10       | ns       |
| $t_{f(c)}$  | Clock fall time (see Figure 2-1)                         | All             |     | 10       | ns       |
| $f_C$       | Clock frequency (see Figure 2-1)                         | TS68C000-8      | 4.0 | 8.0      | MHz      |
|             |                                                          | TS68C000-10     | 4.0 | 10.0     | MHz      |
|             |                                                          | TS68C000-12     | 4.0 | 12.5     | MHz      |
| $t_{CYC}$   | Clock time (see Figure 2-1)                              | TS68C000-8      | 125 | 250      | ns       |
|             |                                                          | TS68C000-10     | 100 | 250      | ns       |
|             |                                                          | TS68C000-12     | 80  | 250      | ns       |
| $t_{W(CL)}$ | Clock pulse width low (see Figure 2-1)                   | TS68C000-8      | 55  | 125      | ns       |
|             |                                                          | TS68C000-10     | 45  | 125      | ns       |
|             |                                                          | TS68C000-12     | 35  | 125      | ns       |
| $t_{W(CH)}$ | Cycle pulse width high (see Figure 2-1)                  | TS68C000-8      | 55  | 125      | ns       |
|             |                                                          | TS68C000-10     | 45  | 125      | ns       |
|             |                                                          | TS68C000-12     | 35  | 125      | ns       |

Note: 1. Load networks number 1 to 4 as specified in "Test Conditions Specific to the Device" on page 26 (Figure 2-2 and Figure 2-3) gives the maximum loading for the relevant output.

#### 2.4.4.3 Special Recommended Conditions for CMOS Devices

##### 1. CMOS Latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become "latched" in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is Implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded tram voltage transients; others may require no additional circuitry.

## 2. CMOS Applications

- The TS68C000 completely satisfies the input/output drive requirements of CMOS logic devices.
- The HCMOS TS68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS68000. However, the TS68C000 does not offer a "power down" or "halt" mode. The minimum operating frequency of the TS68C000 is 4 MHz.

## 2.4.5 Thermal Characteristics

**Table 2-3.** Thermal Characteristics

| Package | Symbol        | Parameter                              | Value | Unit |
|---------|---------------|----------------------------------------|-------|------|
| DIL 64  | $\theta_{JA}$ | Thermal resistance junction to ambient | 25    | °C/W |
|         | $\theta_{JC}$ | Thermal resistance junction to case    | 6     | °C/W |
| PGA 68  | $\theta_{JA}$ | Thermal resistance junction to ambient | 30    | °C/W |
|         | $\theta_{JC}$ | Thermal resistance junction to case    | 6     | °C/W |
| LCCC 68 | $\theta_{JA}$ | Thermal resistance junction to ambient | 40    | °C/W |
|         | $\theta_{JC}$ | Thermal resistance junction to case    | 8     | °C/W |
| CQFP 68 | $\theta_{JA}$ | Thermal resistance junction to ambient | 40    | °C/W |
|         | $\theta_{JC}$ | Thermal resistance junction to case    | 10    | °C/W |

### 2.4.5.1 Power Considerations

The average chip-junction temperature,  $T_J$ , in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

$T_A$  = Ambient Temperature, °C

$\theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient, °C/W

$$P_D = P_{INT} + P_{I/O}$$

$P_{INT} = I_{CC} \times V_{CC}$ , Watts – Chip Internal Power

$P_{I/O}$  = Power Dissipation on Input and Output Pins – User Determined

For most applications  $P_{I/O} < P_{INT}$  and can be neglected.

An Approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K: (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is constant pertaining to the particular part K can be determined from the equation (3) by measuring PD (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

The total thermal resistance of a package ( $\theta_{JA}$ ) can be separated into two components,  $\theta_{JC}$  and  $\theta_{CA}$ , representing the barrier to heat flow from the semiconductor junction to the package (case), surface ( $\theta_{JC}$ ) and from the case to the outside ambient ( $\theta_{CA}$ ).

These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

$\theta_{JA}$  is device related and cannot be influenced by the user. However,  $\theta_{CA}$  is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce  $\theta_{CA}$  so that  $\theta_{JA}$  approximately equals  $\theta_{JC}$ . Substitution of  $\theta_{JC}$  for  $\theta_{JA}$  in equation (1) will result in a lower semiconductor junction temperature.

#### 2.4.6 Mechanical and Environmental

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

#### 2.4.7 Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of inspection lot
- ESD Identifier if Available
- Country of Manufacturing

### 2.5 Quality Conformance Inspection

#### 2.5.1 DESC/MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

### 2.6 Electrical Characteristics

#### 2.6.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below:

- [Table 2-4](#): Static Electrical Characteristics for all electrical variants.
- [Table 2-5](#), [Table 2-6](#), [Table 2-7](#) and [Table 2-8](#): Dynamic electrical characteristics for 8 MHz, 10 MHz and 12.5 MHz.

For static characteristics ([Table 2-4](#)), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause "[Test Conditions Specific to the Device](#)" on page 26 of this specification ([Table 2-5](#), [Table 2-6](#), [Table 2-7](#) and [Table 2-8](#)).

Indication of "min" or "max" in the column "test temperature" means minimum or maximum operating temperatures as defined in sub-clause "[Recommended Condition of Use and Guaranteed Characteristics](#)" on page 11 here above.

**Table 2-4.** Static Characteristics

 $V_{CC} = 5.0V$   $V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^{\circ}C$  and  $-40^{\circ}C/+85^{\circ}C$ 

| Test Number | Symbol         | Parameter                                                                                                              | Ref Number (**) | Test Conditions                                                                           | Test Temperature | Limits  |                 | Unit    |
|-------------|----------------|------------------------------------------------------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------|------------------|---------|-----------------|---------|
|             |                |                                                                                                                        |                 |                                                                                           |                  | Min (*) | Max (*)         |         |
| 1           | $I_{CC}$       | Supply current                                                                                                         | 41              | $V_{CC} = 5.5V$<br>$F_C = 8\text{ MHz}$<br>$F_C = 10\text{ MHz}$<br>$F_C = 12\text{ MHz}$ | All              |         | 42<br>45<br>50  | mA      |
| 2           | $V_{OL}^{(1)}$ | Low level output voltage for: A1 to A23<br>FC0 to FC2; $\overline{BG}$                                                 | 37              | $V_{CC} = 4.5V$<br><br>$I_{OL} = 3.2\text{ mA}$                                           | 25°C             |         | 0.5             | V       |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 3           | $V_{OL}^{(2)}$ | Low level output voltage for:<br>$\overline{HALT}$                                                                     | 37              | $V_{CC} = 4.5V$<br><br>$I_{OL} = 1.6\text{ mA}$                                           | 25°C             |         | 0.5             | V       |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 4           | $V_{OL}^{(3)}$ | Low level output voltage for:<br>$\overline{AS}$ ; R/W:<br>D0 to D15 UDS;<br>$\overline{LDS}$ ; $\overline{VMA}$ and E | 37              | $V_{CC} = 4.5V$<br><br>$I_{OL} = 5.3\text{ mA}$                                           | 25°C             |         | 0.5             | V       |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 5           | $V_{OL}^{(4)}$ | Low level output voltage for:<br>$\overline{RESET}$                                                                    | 37              | $V_{CC} = 4.5V$<br><br>$I_{OL} = 5.0\text{ mA}$                                           | 25°C             |         | 0.5             | V       |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 6           | $V_{OH}$       | High level output voltage for all outputs                                                                              | 37              | $V_{CC} = 4.5V$<br><br>$I_{OH} = -400\text{ }\mu A$                                       | 25°C             | 2.4     | $V_{CC} - 0.75$ | V       |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 7           | $I_{IH}^{(1)}$ | High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$                              | 38              | $V_{CC} = 5.5V$<br><br>$V_I = 5.5V$                                                       | 25°C             |         | 2.5             | $\mu A$ |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 8           | $I_{IL}^{(1)}$ | Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$                               | 38              | $V_{CC} = 5.5V$<br><br>$V_I = 0V$                                                         | 25°C             | -2.5    |                 | $\mu A$ |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 9           | $I_{IH}^{(2)}$ | High level input current for:<br>$\overline{HALT}$ and $\overline{RESET}$                                              | 38              | $V_{CC} = 5.5V$<br><br>$V_I = 5.5V$                                                       | 25°C             |         | 20              | $\mu A$ |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |
| 10          | $I_{IL}^{(2)}$ | Low level input current for:<br>$\overline{HALT}$ and $\overline{RESET}$                                               | 38              | $V_{CC} = 5.5V$<br><br>$V_I = 0V$                                                         | 25°C             | -20     |                 | $\mu A$ |
|             |                |                                                                                                                        |                 |                                                                                           | max              |         |                 |         |
|             |                |                                                                                                                        |                 |                                                                                           | min              |         |                 |         |

**Table 2-4.** Static Characteristics (Continued)  
 $V_{CC} = 5.0V$   $V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^{\circ}C$  and  $-40^{\circ}C/+85^{\circ}C$

| Test Number | Symbol     | Parameter                                      | Ref Number (**) | Test Conditions                          | Test Temperature | Limits  |         | Unit    |
|-------------|------------|------------------------------------------------|-----------------|------------------------------------------|------------------|---------|---------|---------|
|             |            |                                                |                 |                                          |                  | Min (*) | Max (*) |         |
| 11          | $I_{OHZ}$  | High level output<br>3-state leakage current   |                 | $V_{CC} = 5.5V$<br><br>$V_{OH} = 2.4V$   | 25°C             |         | 20      | $\mu A$ |
|             |            |                                                |                 |                                          | max              |         |         |         |
|             |            |                                                |                 |                                          | min              |         |         |         |
| 12          | $I_{OLZ}$  | Low level output<br>3-state leakage current    |                 | $V_{CC} = 5.5V$<br><br>$V_{OL} = 0.4V$   | 25°C             |         | 20      | $\mu A$ |
|             |            |                                                |                 |                                          | max              |         |         |         |
|             |            |                                                |                 |                                          | min              |         |         |         |
| 13          | $V_{IH}$   | High level input<br>voltage for all inputs     |                 | $V_{CC} = 4.5V$<br><br>$V_{CC} = 5.5V$   | 25°C             | 2.0     |         | V       |
|             |            |                                                |                 |                                          | max              |         |         |         |
|             |            |                                                |                 |                                          | min              |         |         |         |
| 14          | $V_{IL}$   | Low level input<br>voltage for all inputs      |                 | $V_{CC} = 4.5V$<br><br>$V_{CC} = 5.5V$   | 25°C             |         | 0.8     | V       |
|             |            |                                                |                 |                                          | max              |         | 0.8     | V       |
|             |            |                                                |                 |                                          | min              |         | 0.8     | V       |
| 14A         | $C_{IN}$   | Input capacitance<br>(all inputs)              | 11              | Reverse<br>voltage = 0V<br>$f = 1.0$ MHz | 25°C             |         | 25      | pF      |
|             |            |                                                |                 |                                          | max              |         | NA      | pF      |
|             |            |                                                |                 |                                          | min              |         | NA      | pF      |
| 14B         | $C_{OUT}$  | Output capacitance<br>(all inputs)             | 11              | Reverse<br>voltage = 0V<br>$f = 1.0$ MHz | 25°C             |         | 20      | pF      |
|             |            |                                                |                 |                                          | max              |         | NA      | pF      |
|             |            |                                                |                 |                                          | min              |         | NA      | pF      |
| 14C         | $V_{TEST}$ | Internal protection<br>Transient energy rating |                 | See note <sup>(9)</sup><br>5 cycles      | 25°C             | -500    | +500    | V       |

Note: \* Algebraic values

\*\* Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26.

Referred notes are given on page 25.

**Table 2-5.** Dynamic Characteristics – TS68C000-8  
 $V_{CC} = 5.0 V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^{\circ}C$  and  $T_c = -40^{\circ}C/+85^{\circ}C$

| Test Number | Symbol          | Parameter                                          | Figure Number (**) | Test Conditions                                                                                               | Test Temperature | Limits             |         | Unit |
|-------------|-----------------|----------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------|------------------|--------------------|---------|------|
|             |                 |                                                    |                    |                                                                                                               |                  | Min (*)            | Max (*) |      |
| 27          | $t_{SU}$ (D1CL) | Set-up time<br>Data-in to clock low <sup>(1)</sup> | 10 – 11            | See "Input and<br>Output Signals<br>for Dynamic<br>Measurements"<br>on page 29<br>(a) to (c)<br>$f_C = 8$ MHz | 25°C             | 20 <sup>(10)</sup> |         | ns   |
|             |                 |                                                    |                    |                                                                                                               | max              |                    |         |      |
|             |                 |                                                    |                    |                                                                                                               | min              |                    |         |      |

**Table 2-5.** Dynamic Characteristics – TS68C000-8 (Continued)  
 $V_{CC} = 5.0 V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^\circ C$  and  $T_c = -40^\circ C/+85^\circ C$

| Test Number | Symbol                            | Parameter                                                                  | Figure Number (**) | Test Conditions            | Test Temperature | Limits             |                   | Unit |
|-------------|-----------------------------------|----------------------------------------------------------------------------|--------------------|----------------------------|------------------|--------------------|-------------------|------|
|             |                                   |                                                                            |                    |                            |                  | Min (*)            | Max (*)           |      |
| 47          | $t_{SU}$<br>(SDTCL)               | Set-up time<br>$\overline{DTACK}$ low to clock low <sup>(1)</sup>          | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBRCL)               | Set-up time<br>$\overline{BR}$ low to clock low <sup>(1)</sup>             | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBGCL)               | Set-up time<br>$\overline{BGACK}$ low to clock low <sup>(1)</sup>          | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SVPACL)              | Set-up time<br>$\overline{VPA}$ low to clock low <sup>(1)</sup>            | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBERCL)              | Set-up time $\overline{BERR}$<br>low to clock low <sup>(1)</sup>           | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 2           | $t_w$<br>(CL)                     | Clock width low                                                            | 10 – 11            | Idem test 27               | 25°C             | 55 <sup>(10)</sup> | 125               | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 3           | $t_w$<br>(CH)                     | Clock width high                                                           | 10 – 11            | Idem test 27               | 25°C             | 55                 | 125               | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 6A          | $t_{PLH}$<br>$t_{PHL}$<br>(CHFCV) | Propagation time<br>clock high to FC valid                                 | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             |                    | 70                | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSLX)              | Propagation time<br>clock high to $\overline{AS}$ low                      | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 60 <sup>(3)</sup> |      |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSL)               | Propagation time<br>CLK high to $\overline{LDS}$ ,<br>$\overline{UDS}$ low | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 60 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 12          | $t_{PLH}$<br>(CLSH)               | Propagation time<br>CLK low to $\overline{AS}$ high                        | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 70 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |

**Table 2-5.** Dynamic Characteristics – TS68C000-8 (Continued)  
 $V_{CC} = 5.0 V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^{\circ}C$  and  $T_c = -40^{\circ}C/+85^{\circ}C$

| Test Number | Symbol                           | Parameter                                                                  | Figure Number (**) | Test Conditions            | Test Temperature | Limits  |                   | Unit |
|-------------|----------------------------------|----------------------------------------------------------------------------|--------------------|----------------------------|------------------|---------|-------------------|------|
|             |                                  |                                                                            |                    |                            |                  | Min (*) | Max (*)           |      |
| 12          | $t_{PLH}$<br>(CLSH)              | Propagation time<br>CLK low to $\overline{LDS}$ , $\overline{UDS}$<br>high | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70 <sup>(3)</sup> | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 18          | $t_{PLH}$<br>(CHRHX)             | Propagation time<br>CLK high to $R/\overline{W}$ high                      | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70 <sup>(3)</sup> | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 20          | $t_{PHL}$<br>(CHRL)              | Propagation time<br>CLK high to $R/\overline{W}$ low                       | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70 <sup>(3)</sup> | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 23          | $t_{PZL}$<br>$t_{PZH}$<br>(CLDO) | Propagation time<br>CLK low to Data-out<br>valid                           | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70 <sup>(3)</sup> | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 6           | $t_{PZL}$<br>$t_{PZH}$<br>(CLAV) | Propagation time<br>CLK low to Address<br>valid                            | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             |         | 70                | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 32          | $t_{HRRF}$                       | $\overline{RESET}/\overline{HALT}$ input<br>transition time                | 10 – 11            | Idem<br>test 27            | 25°C             |         | 200               | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 33          | $t_{PHL}$<br>(CHGL)              | Propagation time<br>CLK high to $\overline{BG}$ low                        | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             |         | 70                | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 34          | $t_{PLH}$<br>(CHGH)              | Propagation time<br>CLK high to $\overline{BG}$ high                       | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             |         | 70                | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 40          | $t_{PHL}$<br>(CLVM)              | Propagation time<br>CLK low to $\overline{VMA}$ low                        | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70                | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 41          | $t_{PHL}$<br>(CLE)               | Propagation time<br>CLK low to E low                                       | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |         | 70                | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |
| 8           | $t_h$<br>(SHAZ)                  | Hold time CLK high<br>to Address                                           | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             | 0       |                   | ns   |
|             |                                  |                                                                            |                    |                            | max              |         |                   |      |
|             |                                  |                                                                            |                    |                            | min              |         |                   |      |

**Table 2-5.** Dynamic Characteristics – TS68C000-8 (Continued)  
 $V_{CC} = 5.0 V_{DC} \pm 10\%$ ;  $GND = 0 V_{DC}$ ;  $T_c = -55/+125^{\circ}C$  and  $T_c = -40^{\circ}C/+85^{\circ}C$

| Test Number | Symbol               | Parameter                                                                 | Figure Number (**) | Test Conditions            | Test Temperature | Limits            |         | Unit                |
|-------------|----------------------|---------------------------------------------------------------------------|--------------------|----------------------------|------------------|-------------------|---------|---------------------|
|             |                      |                                                                           |                    |                            |                  | Min (*)           | Max (*) |                     |
| 11          | $t_{SU}$<br>(AVSL)   | Set-up time<br>Address valid to<br>AS, LDS, UDS low                       | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             | 30 <sup>(4)</sup> |         | ns                  |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   |         |                     |
| 35          | $t_{PHL}$<br>(BRLGL) | Propagation time<br>$\overline{BR}$ low to<br>$\overline{BG}$ low         | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5     | CLKS <sup>(2)</sup> |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   | +90     | ns                  |
| 37          | $t_{PLH}$<br>(GALEH) | Propagation time<br>$\overline{BGACK}$ low to<br>$\overline{BG}$ high     | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5     | CLKS <sup>(2)</sup> |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   | +90     | ns                  |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>$\overline{BERR}$ low to<br>$\overline{DTACK}$ low         | 11                 | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> | –       | ns                  |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   |         |                     |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>$\overline{BERR}$ low to<br>$\overline{DTACK}$ low         | 10 – 11            | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> | –       | ns                  |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   |         |                     |
| 26          | $t_h$<br>(DOSL)      | Hold time<br>Data-out valid to<br>$\overline{LDS}$ , $\overline{UDS}$ low | 11                 | Idem<br>test 27<br>Load: 4 | 25°C             | 30 <sup>(4)</sup> | –       | ns                  |
|             |                      |                                                                           |                    |                            | max              |                   |         |                     |
|             |                      |                                                                           |                    |                            | min              |                   |         |                     |

Note: \* Algebraic values

\*\* Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

Referred notes are given on page 25.

**Table 2-6.** Dynamic Characteristics – TS68C000-10

| Test Number | Symbol           | Parameter                                                         | Figure Number (**) | Test Conditions                                                                                         | Test Temperature | Limits             |         | Unit |
|-------------|------------------|-------------------------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------|------------------|--------------------|---------|------|
|             |                  |                                                                   |                    |                                                                                                         |                  | Min (*)            | Max (*) |      |
| 27          | $t_{SU}$ (DIDL)  | Set-up time<br>Data-in to clock low <sup>(1)</sup>                | 10 – 11            | See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c)<br>$f_c = 10 \text{ MHz}$ | 25°C             | 20 <sup>(10)</sup> |         | ns   |
|             |                  |                                                                   |                    |                                                                                                         | max              |                    |         |      |
|             |                  |                                                                   |                    |                                                                                                         | min              |                    |         |      |
| 47          | $t_{SU}$ (SDTCL) | Set-up time<br>$\overline{DTACK}$ low to clock low <sup>(1)</sup> | 10 – 11            | Idem test 27                                                                                            | 25°C             | 20 <sup>(10)</sup> |         | ns   |
|             |                  |                                                                   |                    |                                                                                                         | max              |                    |         |      |
|             |                  |                                                                   |                    |                                                                                                         | min              |                    |         |      |

**Table 2-6.** Dynamic Characteristics – TS68C000-10 (Continued)

| Test Number | Symbol                            | Parameter                                                         | Figure Number (**) | Test Conditions            | Test Temperature | Limits             |                   | Unit |
|-------------|-----------------------------------|-------------------------------------------------------------------|--------------------|----------------------------|------------------|--------------------|-------------------|------|
|             |                                   |                                                                   |                    |                            |                  | Min (*)            | Max (*)           |      |
| 47          | $t_{SU}$<br>(SBRCL)               | Set-up time<br>$\overline{BR}$ low to clock low <sup>(1)</sup>    | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBGCL)               | Set-up time<br>$\overline{BGACK}$ low to clock low <sup>(1)</sup> | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SVPACL)              | Set-up time<br>$\overline{VPA}$ low to clock low <sup>(1)</sup>   | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBERCL)              | Set-up time $\overline{BERR}$<br>low to clock low <sup>(1)</sup>  | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 2           | $t_w$<br>(CL)                     | Clock width low                                                   | 10 – 11            | Idem test 27               | 25°C             | 45                 | 125               | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 3           | $t_w$<br>(CH)                     | Clock width high                                                  | 10 – 11            | Idem test 27               | 25°C             | 45                 | 125               | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 6A          | $t_{PLH}$<br>$t_{PHL}$<br>(CHFCV) | Propagation time<br>clock high to FC valid                        | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             |                    | 60                | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSLX)              | Propagation time<br>clock high to AS low                          | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSL)               | Propagation time<br>CLK high to LDS,<br>UDS low                   | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 12          | $t_{PLH}$<br>(CLSH)               | Propagation time<br>CLK low to AS high                            | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |
| 12          | $t_{PLH}$<br>(CLSH)               | Propagation time<br>CLK low to LDS, UDS<br>high                   | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                   |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                   |                    |                            | min              |                    |                   |      |

**Table 2-6.** Dynamic Characteristics – TS68C000-10 (Continued)

| Test Number | Symbol                           | Parameter                                           | Figure Number (**) | Test Conditions            | Test Temperature | Limits            |                   | Unit |
|-------------|----------------------------------|-----------------------------------------------------|--------------------|----------------------------|------------------|-------------------|-------------------|------|
|             |                                  |                                                     |                    |                            |                  | Min (*)           | Max (*)           |      |
| 18          | $t_{PLH}$<br>(CHRHX)             | Propagation time<br>CLK high to R/W high            | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 60 <sup>(3)</sup> | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 20          | $t_{PHL}$<br>(CHRL)              | Propagation time<br>CLK high to R/W low             | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 60 <sup>(3)</sup> | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 23          | $t_{PZL}$<br>$t_{PZH}$<br>(CLDO) | Propagation time<br>CLK low to Data-out<br>valid    | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 55 <sup>(3)</sup> | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 6           | $t_{PZL}$<br>$t_{PZH}$<br>(CLAV) | Propagation time<br>CLK low to Address<br>valid     | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 60                | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 32          | $t_{HRRF}$<br>(CHGL)             | RESET/HALT input<br>transition time                 | 10 – 11            | Idem<br>test 27            | 25°C             |                   | 200               | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 33          | $t_{PHL}$<br>(CHGL)              | Propagation time<br>CLK high to BG low              | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             |                   | 60                | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 34          | $t_{PLH}$<br>(CHGH)              | Propagation time<br>CLK high to BG high             | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             |                   | 60                | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 40          | $t_{PHL}$<br>(CLVM)              | Propagation time<br>CLK low to VMA low              | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 70                | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 41          | $t_{PHL}$<br>(CLE)               | Propagation time<br>CLK low to E low                | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 55                | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 8           | $t_H$<br>(SHAZ)                  | Hold time CLK high<br>to Address                    | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             | 0                 |                   | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |
| 11          | $t_{SU}$<br>(AVSL)               | Set-up time<br>Address valid to<br>AS, LDS, UDS low | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             | 20 <sup>(4)</sup> |                   | ns   |
|             |                                  |                                                     |                    |                            | max              |                   |                   |      |
|             |                                  |                                                     |                    |                            | min              |                   |                   |      |

**Table 2-6.** Dynamic Characteristics – TS68C000-10 (Continued)

| Test Number | Symbol               | Parameter                                      | Figure Number (**) | Test Conditions            | Test Temperature | Limits            |         | Unit        |
|-------------|----------------------|------------------------------------------------|--------------------|----------------------------|------------------|-------------------|---------|-------------|
|             |                      |                                                |                    |                            |                  | Min (*)           | Max (*) |             |
| 35          | $t_{PHL}$<br>(BRLGL) | Propagation time<br>BR low to<br>BG low        | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5     | CLKS<br>(2) |
|             |                      |                                                |                    |                            | max              |                   |         | ns          |
|             |                      |                                                |                    |                            | min              |                   | +80     |             |
| 37          | $t_{PLH}$<br>(GALGH) | Propagation time<br>BGACK low to<br>BG high    | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5     | CLKS<br>(2) |
|             |                      |                                                |                    |                            | max              |                   |         | ns          |
|             |                      |                                                |                    |                            | min              |                   | +80     |             |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>BERR low to<br>DTACK low        | 11                 | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> |         | ns          |
|             |                      |                                                |                    |                            | max              |                   |         |             |
|             |                      |                                                |                    |                            | min              |                   |         |             |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>BERR low to<br>DTACK low        | 10 – 11            | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> |         | ns          |
|             |                      |                                                |                    |                            | max              |                   |         |             |
|             |                      |                                                |                    |                            | min              |                   |         |             |
| 26          | $t_H$<br>(DOSL)      | Hold time<br>Data-out valid to<br>LDS, UDS low | 11                 | Idem<br>test 27<br>Load: 4 | 25°C             | 20 <sup>(4)</sup> |         | ns          |
|             |                      |                                                |                    |                            | max              |                   |         |             |
|             |                      |                                                |                    |                            | min              |                   |         |             |

Note: \* Algebraic values

\*\* Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

Referred notes are given on page 25.

**Table 2-7.** Dynamic Characteristics – TS68C000-12

| Test Number | Symbol              | Parameter                                               | Figure Number (**) | Test Conditions                                                                                                | Test Temperature | Limits             |         | Unit |
|-------------|---------------------|---------------------------------------------------------|--------------------|----------------------------------------------------------------------------------------------------------------|------------------|--------------------|---------|------|
|             |                     |                                                         |                    |                                                                                                                |                  | Min (*)            | Max (*) |      |
| 27          | $t_{SU}$ (DIDL)     | Set-up time<br>Data-in to clock<br>low <sup>(1)</sup>   | 10 – 11            | See "Input and<br>Output Signals for<br>Dynamic<br>Measurements" on<br>page 29<br>(a) to (c)<br>$f_C = 12$ MHz | 25°C             | 10 <sup>(10)</sup> |         | ns   |
|             |                     |                                                         |                    |                                                                                                                | max              |                    |         |      |
|             |                     |                                                         |                    |                                                                                                                | min              |                    |         |      |
| 47          | $t_{SU}$<br>(SDTCL) | Set-up time<br>DTACK low to<br>clock low <sup>(1)</sup> | 10 – 11            | Idem test 27                                                                                                   | 25°C             | 20 <sup>(10)</sup> |         | ns   |
|             |                     |                                                         |                    |                                                                                                                | max              |                    |         |      |
|             |                     |                                                         |                    |                                                                                                                | min              |                    |         |      |
| 47          | $t_{SU}$<br>(SBRCL) | Set-up time<br>BR low to clock<br>low <sup>(1)</sup>    | 10 – 11            | Idem test 27                                                                                                   | 25°C             | 20 <sup>(10)</sup> |         | ns   |
|             |                     |                                                         |                    |                                                                                                                | max              |                    |         |      |
|             |                     |                                                         |                    |                                                                                                                | min              |                    |         |      |

**Table 2-7.** Dynamic Characteristics – TS68C000-12 (Continued)

| Test Number | Symbol                            | Parameter                                                                  | Figure Number (**) | Test Conditions            | Test Temperature | Limits             |                   | Unit |
|-------------|-----------------------------------|----------------------------------------------------------------------------|--------------------|----------------------------|------------------|--------------------|-------------------|------|
|             |                                   |                                                                            |                    |                            |                  | Min (*)            | Max (*)           |      |
| 47          | $t_{SU}$<br>(SBGCL)               | Set-up time<br>$\overline{BGACK}$ low to clock low <sup>(1)</sup>          | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SVPACL)              | Set-up time<br>$\overline{VPA}$ low to clock low <sup>(1)</sup>            | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 47          | $t_{SU}$<br>(SBERCL)              | Set-up time $\overline{BERR}$<br>low to clock low <sup>(1)</sup>           | 10 – 11            | Idem test 27               | 25°C             | 20 <sup>(10)</sup> |                   | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 2           | $t_w$<br>(CL)                     | Clock width low                                                            | 10 – 11            | Idem test 27               | 25°C             | 35                 | 125               | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 3           | $t_w$<br>(CH)                     | Clock width high                                                           | 10 – 11            | Idem test 27               | 25°C             | 35                 | 125               | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 6A          | $t_{PLH}$<br>$t_{PHL}$<br>(CHFCV) | Propagation time<br>clock high to FC<br>valid                              | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             |                    | 55                | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSLX)              | Propagation time<br>clock high to $\overline{AS}$<br>low                   | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 9           | $t_{PHL}$<br>(CHSL)               | Propagation time<br>CLK high to $\overline{LDS}$ ,<br>$\overline{UDS}$ low | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 55 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 12          | $t_{PLH}$<br>(CLSH)               | Propagation time<br>CLK low to $\overline{LDS}$ ,<br>$\overline{UDS}$ high | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 50 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 12          | $t_{PLH}$<br>(CLSH)               | Propagation time<br>CLK low to $\overline{LDS}$ ,<br>$\overline{UDS}$ high | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 50 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |
| 18          | $t_{PLH}$<br>(CHRHX)              | Propagation time<br>CLK high to R/W<br>high                                | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                    | 60 <sup>(3)</sup> | ns   |
|             |                                   |                                                                            |                    |                            | max              |                    |                   |      |
|             |                                   |                                                                            |                    |                            | min              |                    |                   |      |

**Table 2-7.** Dynamic Characteristics – TS68C000-12 (Continued)

| Test Number | Symbol                           | Parameter                                                                                                         | Figure Number (**) | Test Conditions            | Test Temperature | Limits            |                   | Unit                |
|-------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------|--------------------|----------------------------|------------------|-------------------|-------------------|---------------------|
|             |                                  |                                                                                                                   |                    |                            |                  | Min (*)           | Max (*)           |                     |
| 20          | $t_{PHL}$<br>(CHRL)              | Propagation time<br>CLK high to R/W<br>low                                                                        | 11                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 60 <sup>(3)</sup> | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 23          | $t_{PZL}$<br>$t_{PZH}$<br>(CLDO) | Propagation time<br>CLK low to Data-<br>out valid                                                                 | 11                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 55 <sup>(3)</sup> | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 6           | $t_{PZL}$<br>$t_{PZH}$<br>(CLAV) | Propagation time<br>CLK low to<br>Address valid                                                                   | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 55                | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 32          | $t_{HRRF}$                       | $\overline{\text{RESET}}/\overline{\text{HALT}}$<br>transition time                                               | 10 – 11            | Idem<br>test 27            | 25°C             |                   | 150               | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 33          | $t_{PHL}$<br>(CHGL)              | Propagation time<br>CLK high to $\overline{\text{BG}}$<br>low                                                     | 8 – 9              | Idem<br>test 27<br>Load: 3 | 25°C             |                   | 50                | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 34          | $t_{PLH}$<br>(CHGH)              | Propagation time<br>CLK high to $\overline{\text{BG}}$<br>high                                                    | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             |                   | 50                | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 40          | $t_{PHL}$<br>(CLVM)              | Propagation time<br>CLK low to $\overline{\text{VMA}}$<br>low                                                     | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 70                | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 41          | $t_{PHL}$<br>(CLE)               | Propagation time<br>CLK low to E low                                                                              | 13                 | Idem<br>test 27<br>Load: 4 | 25°C             |                   | 45                | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 8           | $t_H$<br>(SHAZ)                  | Hold time CLK<br>high to Address                                                                                  | 10 – 11            | Idem<br>test 27<br>Load: 3 | 25°C             | 0                 |                   | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 11          | $t_{SU}$<br>(AVSL)               | Set-up time<br>Address valid to<br>$\overline{\text{AS}}$ , $\overline{\text{LDS}}$ , $\overline{\text{UDS}}$ low | 10 – 11            | Idem<br>test 27<br>Load: 4 | 25°C             | 15 <sup>(4)</sup> |                   | ns                  |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   |                     |
|             |                                  |                                                                                                                   |                    |                            | min              |                   |                   |                     |
| 35          | $t_{PHL}$<br>(BRLGL)             | Propagation time<br>$\overline{\text{BR}}$ low to<br>$\overline{\text{BG}}$ low                                   | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5               | CLKS <sup>(2)</sup> |
|             |                                  |                                                                                                                   |                    |                            | max              |                   |                   | ns                  |
|             |                                  |                                                                                                                   |                    |                            | min              |                   | +70               | ns                  |

**Table 2-7.** Dynamic Characteristics – TS68C000-12 (Continued)

| Test Number | Symbol               | Parameter                                                                 | Figure Number (**) | Test Conditions            | Test Temperature | Limits            |         | Unit              |
|-------------|----------------------|---------------------------------------------------------------------------|--------------------|----------------------------|------------------|-------------------|---------|-------------------|
|             |                      |                                                                           |                    |                            |                  | Min (*)           | Max (*) |                   |
| 37          | $t_{PLH}$<br>(GALGH) | Propagation time<br>$\overline{BGACK}$ low to<br>$\overline{BG}$ high     | 12                 | Idem<br>test 27<br>Load: 3 | 25°C             | 1.5               | 3.5     | CLKS<br>(2)<br>ns |
|             |                      |                                                                           |                    |                            | max              |                   |         |                   |
|             |                      |                                                                           |                    |                            | min              |                   | +70     |                   |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>$\overline{BERR}$ low to<br>$\overline{DTACK}$ low         | 11                 | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> |         | ns                |
|             |                      |                                                                           |                    |                            | max              |                   |         |                   |
|             |                      |                                                                           |                    |                            | min              |                   |         |                   |
| 48          | $t_{SU}$<br>(BELDAL) | Set-up time<br>$\overline{BERR}$ low to<br>$\overline{DTACK}$ low         | 10 – 11            | Idem<br>test 27            | 25°C             | 20 <sup>(5)</sup> |         | ns                |
|             |                      |                                                                           |                    |                            | max              |                   |         |                   |
|             |                      |                                                                           |                    |                            | min              |                   |         |                   |
| 26          | $t_H$<br>(DOSL)      | Hold time<br>Data-out valid to<br>$\overline{LDS}$ , $\overline{UDS}$ low | 11                 | Idem<br>test 27<br>Load: 4 | 25°C             | 15 <sup>(4)</sup> |         | ns                |
|             |                      |                                                                           |                    |                            | max              |                   |         |                   |
|             |                      |                                                                           |                    |                            | min              |                   |         |                   |

Note: \* Algebraic values

\*\* Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

**2.6.1.1** Referred notes to [Table 2-4](#), [Table 2-5](#), [Table 2-6](#), [Table 2-7](#)

The following notes shall apply where referred into [Table 2-4](#), [Table 2-5](#), [Table 2-6](#) and [Table 2-7](#).

- Notes:
1. If the asynchronous setup time (47) requirements are satisfied, the  $\overline{DTACK}$  low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
  2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
  3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
  4. Actual value depends on period.
  5. If 47 is satisfied for both  $\overline{DTACK}$  and  $\overline{BERR}$ , 48 may be 0 nanoseconds.
  6. The processor will negate  $\overline{BG}$  and begin driving the bus again if external arbitration logic negates  $\overline{BR}$  before asserting  $\overline{BGACK}$ .
  7. The falling edge of 56 triggers both the negation of the strobes ( $\overline{AS}$ , and  $\overline{XDS}$ ) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
  8. When  $\overline{AS}$  and  $\overline{R/W}$  are equally loaded ( $\pm 20\%$ ), substrate 10 nanoseconds from the values in these columns.
  9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in [Table 2-5](#), [Table 2-6](#) and [Table 2-7](#).
  10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.

**Table 2-8.** AC Electrical Specification – Clock Timing

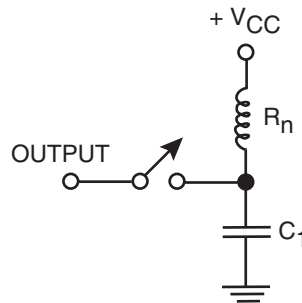
| Symbol                             | Parameter              | 8 MHz    |            | 10 MHz   |            | 12.5 MHz |            | Unit |
|------------------------------------|------------------------|----------|------------|----------|------------|----------|------------|------|
|                                    |                        | Min      | Max        | Min      | Max        | Min      | Max        |      |
| f                                  | Frequency of operation | 4.0      | 8.0        | 4.0      | 10.0       | 4.0      | 12.5       | MHz  |
| t <sub>cyc</sub>                   | Cycle time             | 125      | 250        | 100      | 250        | 80       | 250        | ns   |
| t <sub>CL</sub><br>t <sub>CH</sub> | Clock pulse width      | 55<br>55 | 125<br>125 | 45<br>45 | 125<br>125 | 35<br>35 | 125<br>125 | ns   |
| t <sub>Cr</sub><br>t <sub>Cf</sub> | Rise and fall times    |          | 10<br>10   |          | 10<br>10   |          | 10<br>10   | ns   |

## 2.6.2 Test Conditions Specific to the Device

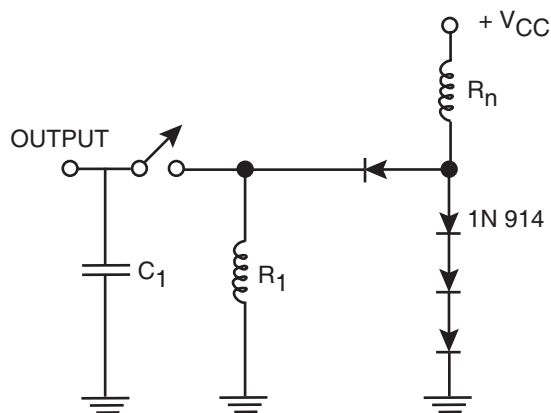
### 2.6.2.1 Loading Network

The applicable loading network shall be as defined in column "Test Conditions" of [Table 2-5](#), [Table 2-6](#) and [Table 2-7](#), referring to the loading network number as shown in [Figure 2-2](#) and [Figure 2-3](#) below.

**Figure 2-2.** Passive Loads



**Figure 2-3.** Active Loads



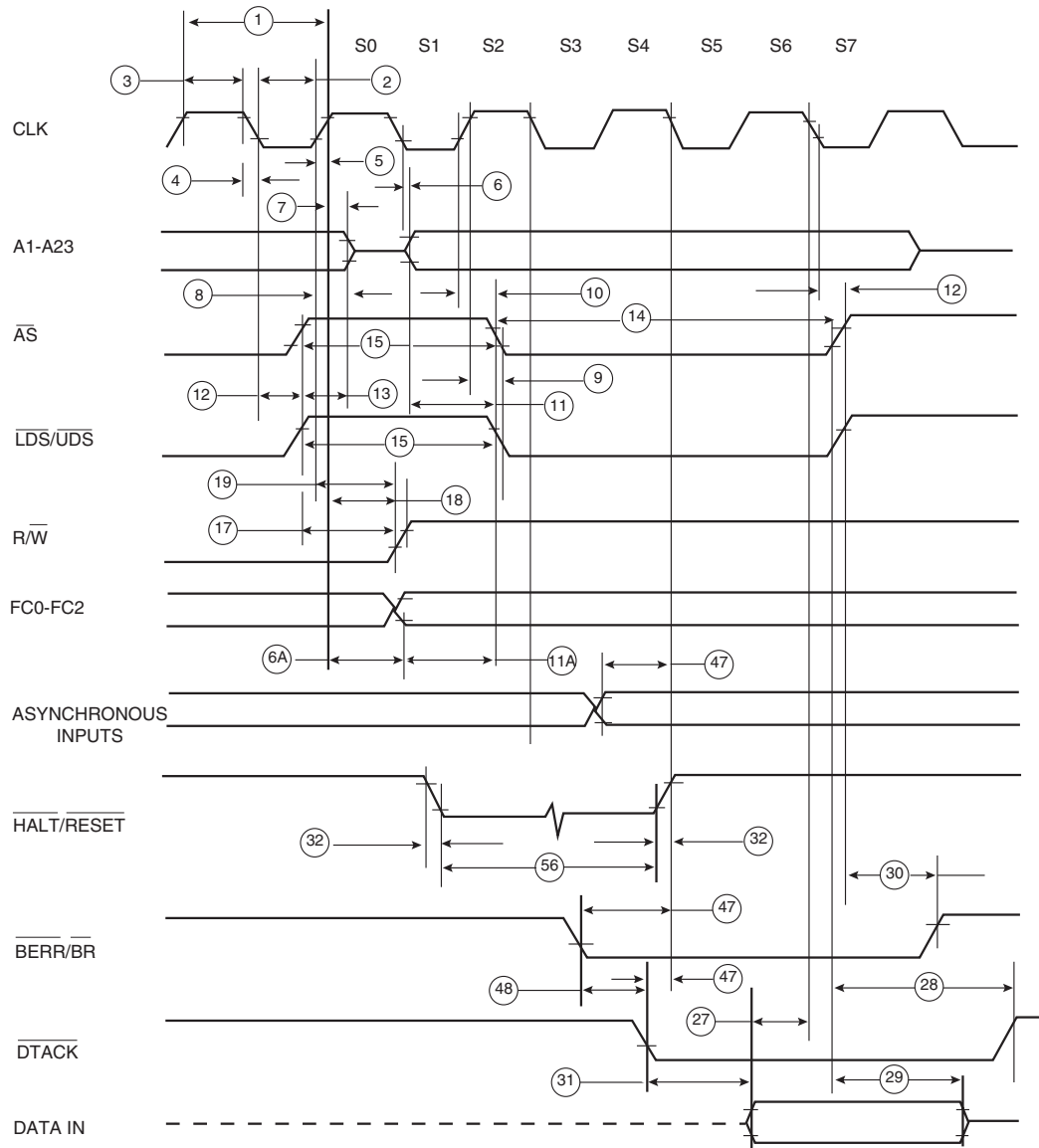
| Load NBR | Figure | R1    | Rn      | C <sub>1</sub> <sup>(1)</sup> | Output Application                               |
|----------|--------|-------|---------|-------------------------------|--------------------------------------------------|
| 1        | 5.1    | —     | 910Ω    | 130 pF                        | $\overline{\text{RESET}}$                        |
| 2        | 5.1    | —     | 2.9 kΩ  | 70 pF                         | $\overline{\text{HALT}}$                         |
| 3        | 5.2    | 6.0 k | 1.22 kΩ | 130 pF                        | A1 to A23, $\overline{\text{BG}}$ and FC0 to FC2 |
| 4        | 5.2    | 6.0 k | 740Ω    | 130 pF                        | All other outputs                                |

Note: 1. C<sub>1</sub> includes all parasitic capacitances of test machines

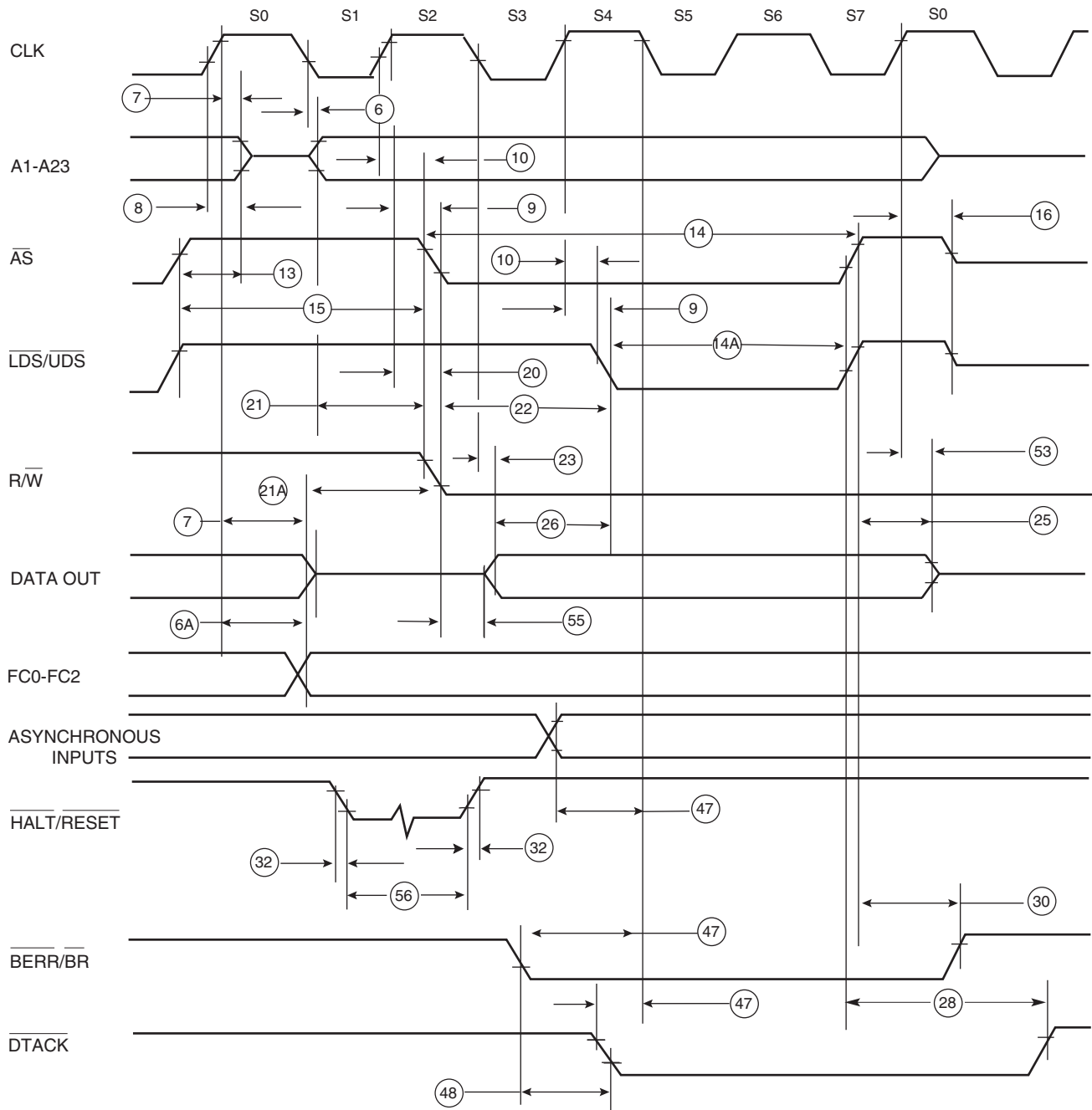
### 2.6.2.2 Time Definitions

The times specified in Table 2-5, Table 2-6 and Table 2-7 as dynamic characteristics are defined in Figure 2-4 to Figure 2-7 below by a reference number given in the column "Method" of the tables together with the relevant figure number.

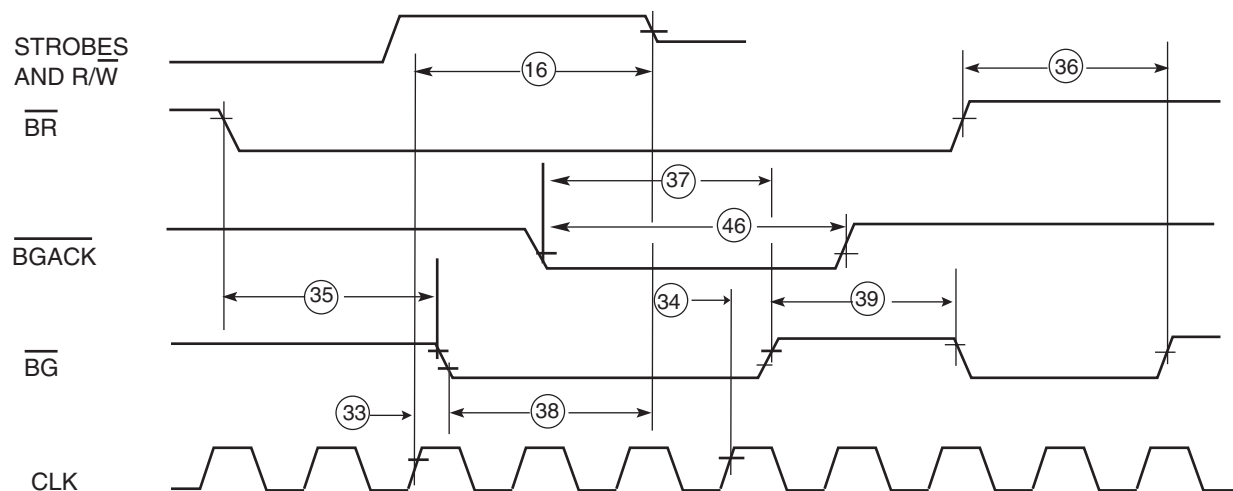
**Figure 2-4.** Read Cycle Timing



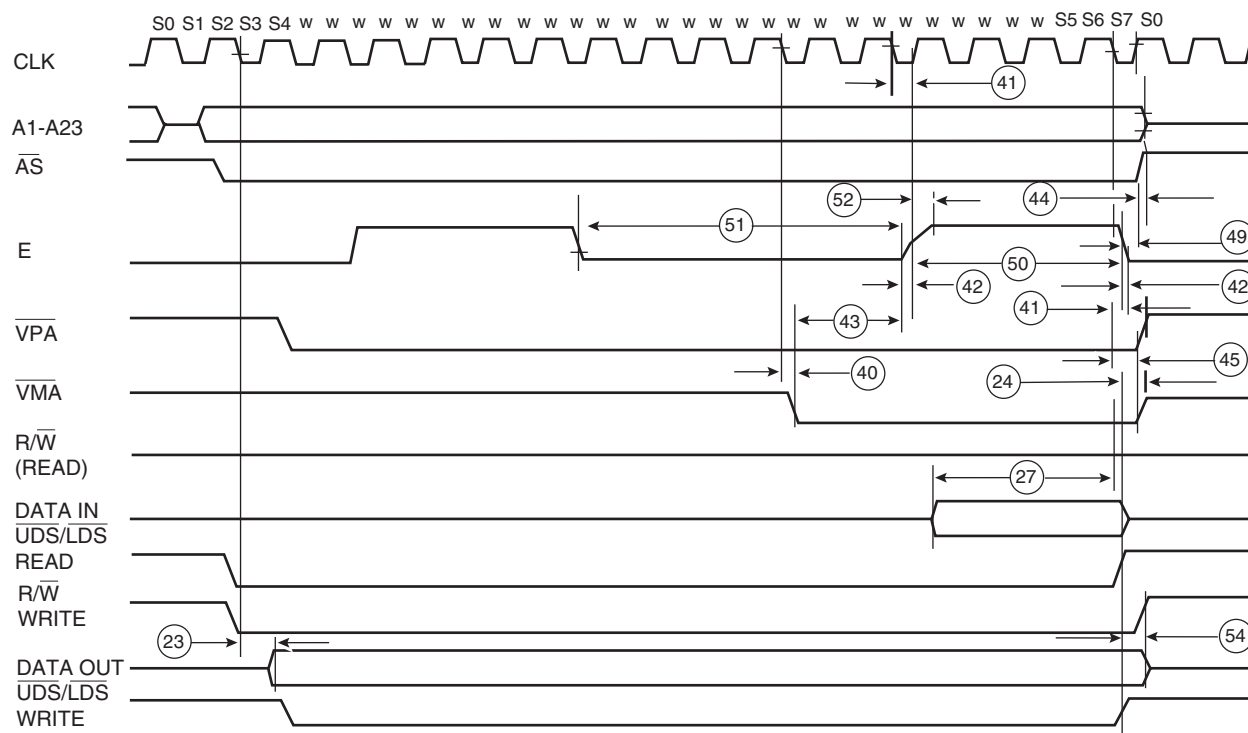
**Figure 2-5. Write Cycle Timing**



**Figure 2-6.** AC Electrical Waveforms – Bus Arbitration



**Figure 2-7.** Enable/Interface Timing

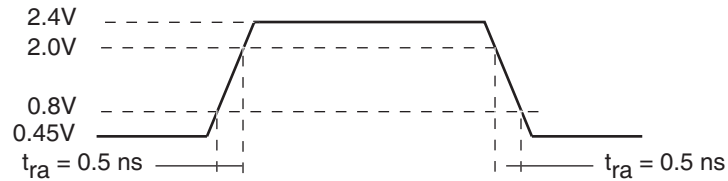


### 2.6.2.3 Input and Output Signals for Dynamic Measurements

#### 1. Input pulse characteristics

Where input pulse generator is loaded by only a 50Ω resistor, the input pulse characteristics shall be as shown in [Figure 2-8](#).

**Figure 2-8.** Input Pulse Characteristics



2. Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be:

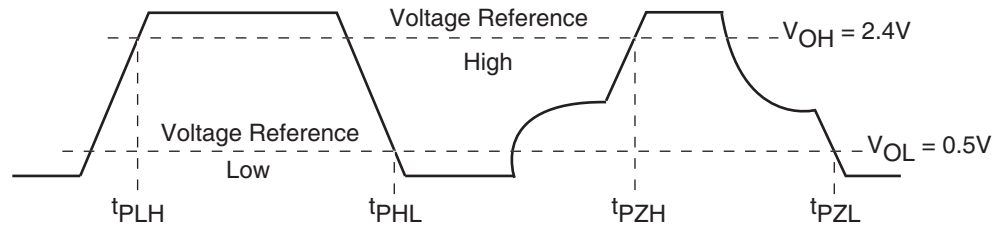
$$V_{IL} = 0.8V$$

$$V_{IH} = 2.0V$$

3. Time measurement input voltage references

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in [Figure 2-9](#).

**Figure 2-9.** Output Voltage References



### 2.6.3 Additional Information

Additional information shall not be for any inspection purposes.

#### 2.6.3.1 Power Considerations

See ["Thermal Characteristics"](#) on page 13.

#### 2.6.3.2 Additional Electrical Characteristics

The following additional characteristics, which are obtained from circuit design, are given for Information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to [Figure 2-1](#) to [Figure 2-7](#) and loading number refer to [Figure 2-2](#) and [Figure 2-3](#) (see ["Test Conditions Specific to the Device"](#) on page 26 of this specification).

The given limits should be valid for all operating temperature ranges as defined in ["Recommended Condition of Use and Guaranteed Characteristics"](#) on page 11 of this specification.

**Table 2-9.** Additional Electrical Characteristics

| Item NO. | Symbol                                          | Parameter                                                                                  | Ref Number         | Load Number | TS68C000-8 |                       | TS68C000-10 |                       | TS68C000-12 |                       | Unit              |
|----------|-------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------|-------------|------------|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------------|
|          |                                                 |                                                                                            |                    |             | Limits     |                       | Limits      |                       | Limits      |                       |                   |
|          |                                                 |                                                                                            |                    |             | Min        | Max                   | Min         | Max                   | Min         | Max                   |                   |
| 6A       | V <sub>OH</sub>                                 | High level output voltage for E with pull up R = 1.1K to V <sub>CC</sub>                   |                    |             | Min        | V <sub>CC</sub> -0.75 | Min         | V <sub>CC</sub> -0.75 | Min         | V <sub>CC</sub> -0.75 | V                 |
| 37       | t <sub>PLZ</sub><br>t <sub>PHZ</sub><br>(CLAZX) | Propagation time CLK low to Address 3-state                                                | Fig. 10<br>Ref. 7  | 3           |            | 80                    |             | 70                    |             | 60                    | ns                |
| 39       | t <sub>PHZ</sub><br>(CHSZX)                     | Propagation time CLK high to $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ 3-state | Fig. 11<br>Ref. 16 | 4           |            | 80                    |             | 70                    |             | 60                    | ns                |
| 40       | t <sub>PLZ</sub><br>t <sub>PHZ</sub><br>(CHRX)  | Propagation time CLK high to R/ $\overline{W}$ 3-state                                     | Fig. 12<br>Ref. 16 | 4           |            | 80                    |             | 70                    |             | 60                    | ns                |
| 41       | t <sub>PHZ</sub><br>t <sub>PLZ</sub><br>(CHAZX) | Propagation time CLK high to Data 3-state                                                  | Fig. 11<br>Ref. 7  | 4           |            | 80                    |             | 70                    |             | 60                    | ns                |
| 43       | t <sub>H</sub><br>(SHAZ)                        | Hold time $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ high to Address            | Fig. 10<br>Ref. 13 | 3           | 30         |                       | 20          |                       | 10          |                       | ns                |
| 44       | t <sub>w</sub><br>(SL)                          | $\overline{AS}/DS$ width low                                                               | Fig. 10<br>Ref. 14 |             | 240<br>(4) |                       | 195<br>(4)  |                       | 160<br>(4)  |                       | ns                |
| 45       | t <sub>w</sub><br>(SL)                          | $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ width high                           | Fig. 10<br>Ref. 15 |             | 150<br>(4) |                       | 105<br>(4)  |                       | 65<br>(4)   |                       | ns                |
| 46       | t <sub>SU</sub><br>(SHRH)                       | Set-up time $\overline{LDS}$ , $\overline{UDS}$ high to R/ $\overline{W}$ high             | Fig. 10<br>Ref. 17 | 4           | 40<br>(4)  |                       | 20<br>(4)   |                       | 10<br>(4)   |                       | ns                |
| 47       | t <sub>SU</sub><br>(AVRL)                       | Set-up time Address valid to R/ $\overline{W}$ low                                         | Fig. 10<br>Ref. 21 | 4           | 20<br>(4)  |                       | 0<br>(4)    |                       | 0<br>(4)    |                       | ns                |
| 48       | t <sub>PHL</sub><br>(RLSL)                      | Propagation time R/ $\overline{W}$ low to I <sub>ds</sub> , u <sub>ds</sub> low            | Fig. 11<br>Ref. 22 | 4           | 80<br>(4)  |                       | 50<br>(4)   |                       | 30<br>(4)   |                       | ns                |
| 49       | t <sub>H</sub><br>(SHDO)                        | Hold time $\overline{LDS}$ , $\overline{UDS}$ high to Data-out                             | Fig. 11<br>Ref. 25 | 4           | 30<br>(4)  |                       | 20<br>(4)   |                       | 15<br>(4)   |                       | ns                |
| 50       | t <sub>H</sub> (SHDI)                           | Hold time $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ high to Data-in            | Fig. 10<br>Ref. 29 |             | 0          |                       | 0           |                       | 0           |                       | ns                |
| 52       | t <sub>H</sub><br>(BRHGH)                       | Propagation time $\overline{BR}$ high to $\overline{BG}$ high <sup>(6)</sup>               | Fig. 12<br>Ref. 36 | 3           | 1.5        | 3.5 + 90              | 1.5         | 3.5 + 80              | 1.5         | 3.5 + 70              | CLKS<br>(2)<br>ns |

**Table 2-9.** Additional Electrical Characteristics (Continued)

| Item NO. | Symbol                          | Parameter                                                                          | Ref Number                                                                                                                                                                     | Load Number                | TS68C000-8 |                    | TS68C000-10 |                    | TS68C000-12 |                    | Unit        |
|----------|---------------------------------|------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|
|          |                                 |                                                                                    |                                                                                                                                                                                |                            | Limits     |                    | Limits      |                    | Limits      |                    |             |
|          |                                 |                                                                                    |                                                                                                                                                                                |                            | Min        | Max                | Min         | Max                | Min         | Max                |             |
| 54       | $t_{PHZ}$<br>$t_{PLZ}$<br>(GLZ) | Propagation time $\overline{BG}$ low to Data and Address 3-state                   | Fig. 12<br>Ref. 36                                                                                                                                                             | BG,<br>address 3<br>Data 4 |            | 80                 |             | 70                 |             | 60                 | ns          |
| 55       | $t_w$ (GH)                      | $\overline{BG}$ width high                                                         | Fig. 12<br>Ref. 39                                                                                                                                                             |                            | 1.5        |                    | 1.5         |                    | 1.5         |                    | CLKS<br>ns  |
| 56       | $t_{PLH}$<br>(VMLEH)            | Propagation time $\overline{VMA}$ low to E high                                    | Fig. 13<br>Ref. 43                                                                                                                                                             | 4                          | 200        |                    | 150         |                    | 90          |                    | ns          |
| 57       | $t_H$<br>(SHVPH)                | Hold time $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ high to VPA high   | Fig. 20 Ref. 44<br>(see "Although UDS and LDS are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally)." on page 45) | 4                          | 0          | 120                | 0           | 90                 | 0           | 70                 | ns          |
| 58       | $t_H$ (ELAI)                    | Hold time E low to address                                                         | Fig. 13<br>Ref. 45                                                                                                                                                             | 3                          | 30         |                    | 10          |                    | 10          |                    | ns          |
| 59       | $t_w$ (BGL)                     | $\overline{BGACK}$ width low                                                       | Fig. 12<br>Ref. 46                                                                                                                                                             |                            | 1.5        |                    | 1.5         |                    | 1.5         |                    | CLKS<br>(2) |
| 61       | $t_w$ (EH)                      | E width high                                                                       | Fig. 13<br>Ref. 50                                                                                                                                                             |                            | 450        |                    | 350         |                    | 280         |                    | ns          |
| 62       | $t_w$ (EL)                      | E width low                                                                        | Fig. 13<br>Ref. 51                                                                                                                                                             |                            | 700        |                    | 550         |                    | 440         |                    | ns          |
| 63       | $t_{PHL}$<br>(FCVSL)            | Propagation time FC valid to $\overline{AS}$ , $\overline{DS}$ low                 | Fig. 10<br>Ref. 1A or 11A                                                                                                                                                      | 4                          | 60<br>(4)  |                    | 50<br>(4)   |                    | 40<br>(4)   |                    | ns          |
| 64       | $t_{PHL}$<br>(SHDAH)            | Propagation time $\overline{AS}$ , $\overline{DS}$ high to $\overline{DTACK}$ high | Fig. 10<br>Ref. 28                                                                                                                                                             | 4                          | 0          | 245 <sup>(4)</sup> | 0           | 190 <sup>(4)</sup> | 0           | 150 <sup>(4)</sup> | ns          |
| 65       | $t_{PLH}$<br>(SHBEH)            | Propagation time $\overline{AS}$ , $\overline{DS}$ high to $\overline{BERR}$ high  | Fig. 12<br>Ref. 30                                                                                                                                                             | 4                          | 0          |                    | 0           |                    | 0           |                    | ns          |
| 66       | $t_{SU}$<br>(DALDI)             | Set-up time $\overline{DTACK}$ low to Data-in <sup>(1)</sup>                       | Fig. 10<br>Ref. 31                                                                                                                                                             |                            |            | 90 <sup>(4)</sup>  |             | 65 <sup>(4)</sup>  |             | 50 <sup>(4)</sup>  | ns          |

**Table 2-9.** Additional Electrical Characteristics (Continued)

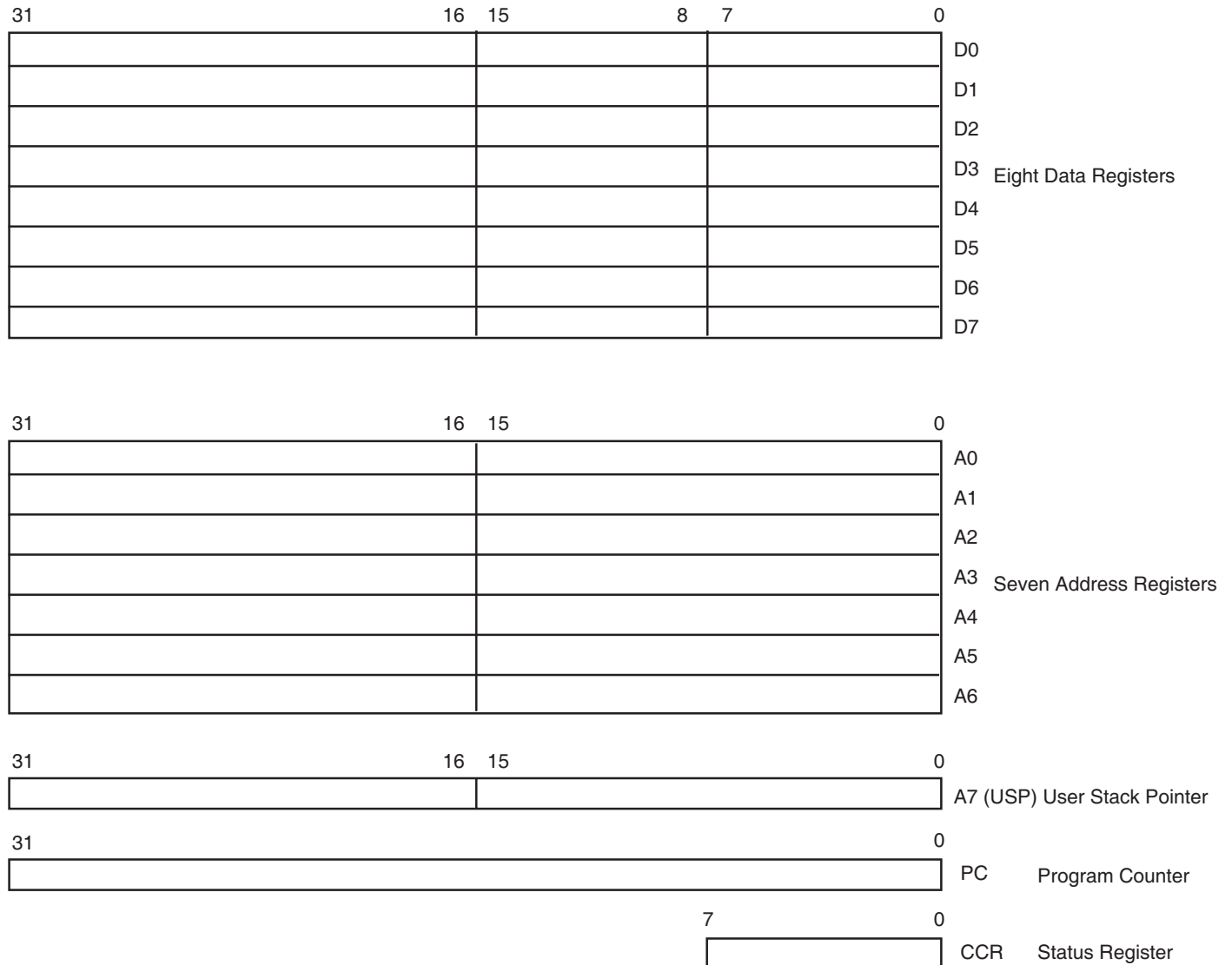
| Item NO. | Symbol                         | Parameter                                                           | Ref Number          | Load Number      | TS68C000-8 |                   | TS68C000-10 |                   | TS68C000-12 |                   | Unit        |
|----------|--------------------------------|---------------------------------------------------------------------|---------------------|------------------|------------|-------------------|-------------|-------------------|-------------|-------------------|-------------|
|          |                                |                                                                     |                     |                  | Limits     |                   | Limits      |                   | Limits      |                   |             |
|          |                                |                                                                     |                     |                  | Min        | Max               | Min         | Max               | Min         | Max               |             |
| 67       | $t_{THL} \ t_{TLH}$<br>(RH)    | Transition time $\overline{HALT}$ , $\overline{RESET}$ input        | Fig. 10<br>Ref. 32  |                  |            | 200               |             | 200               |             | 200               | ns          |
| 69       | $t_w$<br>(HRPW)                | $\overline{HALT}$ and $\overline{RESET}$ pulse width after power up | Fig. 10<br>Ref. 56  |                  | 10         |                   | 10          |                   | 10          |                   | CLKS<br>(2) |
| 70       | $t_{PHL}$<br>(ASRV)            | Propagation time $\overline{AS}$ low to $R/\overline{W}$ valid      | Fig. 11<br>Ref. 20A | 4                |            | 20 <sup>(8)</sup> |             | 20 <sup>(8)</sup> |             | 20 <sup>(8)</sup> | ns          |
| 71       | $t_{PHL}$<br>(FCVRL)           | Propagation time FC valid to $R/\overline{W}$ low                   | Fig. 11<br>Ref. 21A | 4                | 60<br>(4)  |                   | 50<br>(4)   |                   | 30<br>(4)   |                   | ns          |
| 73       | $t_H$<br>(CHDOI)               | Hold time CLK high to Data-out                                      | Fig. 11<br>Ref. 53  | 4                | 0          |                   | 0           |                   | 0           |                   | ns          |
| 74       | $t_{PLH} \ t_{PHL}$<br>(RLDBO) | Propagation time $R/\overline{W}$ low to Data-bus impedance change  | Fig. 11<br>Ref. 55  | 4                | 30         |                   | 20          |                   | 10          |                   | ns          |
| 75       | $t_{PHL}$<br>(SHEL)            | Propagation time $\overline{AS}$ , $\overline{DS}$ low to E low     | Fig. 13<br>Ref. 49  | 4 <sup>(7)</sup> | -70        | +70               | -55         | +55               | -45         | +45               | ns          |
| 76       | $t_H$<br>(ELDOI)               | Hold time E low to Data-out                                         | Fig. 13<br>Ref. 54  | 4                | 30         |                   | 20          |                   | 15          |                   | ns          |

- Notes:
1. If the asynchronous setup time (47) requirements are satisfied, the  $\overline{DTACK}$  low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
  2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
  3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
  4. Actual value depends on period.
  5. If 47 is satisfied for both  $\overline{DTACK}$  and  $\overline{BERR}$ , 48 may be 0 nanoseconds.
  6. The processor will negate  $\overline{BG}$  and begin driving the bus again if external arbitration logic negates  $\overline{BR}$  before asserting  $\overline{BGACK}$ .
  7. The falling edge of 56 triggers both the negation of the strobes ( $\overline{AS}$ , and X  $\overline{DS}$ ) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
  8. When  $\overline{AS}$  and  $R/\overline{W}$  are equally loaded ( $\pm 20\%$ ), substrate 10 nanoseconds from the values in these columns.
  9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in Table 2-5, Table 2-6 and Table 2-7.
  10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.

## 2.7 Functional Description

### 2.7.1 Description of Registers

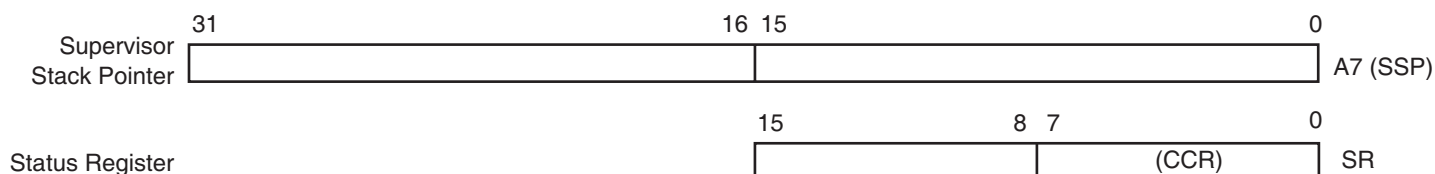
**Figure 2-10.** User Programming Model



As shown in the user programming model ([Figure 2-10](#)), the TS68C000 offers 16/32 bits registers and a 32 bits program counter. The first eight registers (D0 – D7) are used as data registers for byte (8-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 16 registers may be used as index registers.

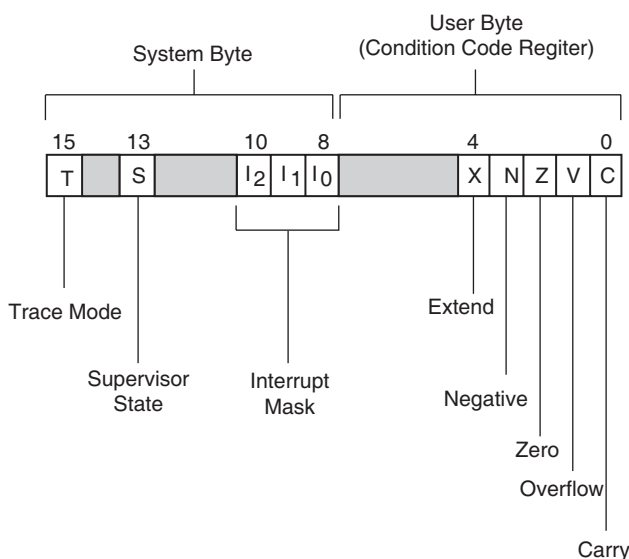
In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in [Figure 2-11](#).

**Figure 2-11.** Supervisor Programming Model Supplement



The status register ([Figure 2-12](#)) contains the interrupt mask (eight levels available) as well as the conditions codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

**Figure 2-12.** Status Register



## 2.7.2 Data Types and Addressing Modes

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status word data, etc. are provided in the instruction set.

The 14 addressing modes, shown in [Table 2-10](#), include six basic types:

- Register Direct
- Register Indirect
- Absolute
- program Counter Relative
- Immediate
- Implied

Included in the register indirect addressing modes is the capability to do post incrementing, pre-decrementing, offsetting, and indexing. The program counter relative mode can also be modified via Indexing and offsetting.

### 2.7.3 Data Transfer Operations

Transfer of data between devices involves the following leads:

1. address bus A1 through A23,
2. data bus 00 through D15, and
3. control signals.

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the TC68C000 for interlocked multiprocessor communications.

#### 2.7.3.1 Read Cycle

During a read cycle, the processor receives data from the memory of a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal AO bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the AO bit equals zero, the upper data strobe is issued. When the AO bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

#### 2.7.3.2 Write Cycle

During a write cycle, the processor sends data to either the memory of a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the AO bit equals zero, the upper data strobe is issued. When the AO bit equals one, the lower data strobe is issued.

**Table 2-10.** Addressing Modes

| Addressing Modes                                                                          | Syntax                                          |
|-------------------------------------------------------------------------------------------|-------------------------------------------------|
| Register direct addressing<br>Data register direct<br>Address register direct             | Dn<br>An                                        |
| Absolute data addressing<br>Absolute short<br>Absolute long                               | xxx.W<br>xxx.L                                  |
| Program counter relative addressing<br>Relative with offset<br>Relative with index offset | d <sub>16</sub> (PC)<br>d <sub>8</sub> (PC, Xn) |

**Table 2-10.** Addressing Modes (Continued)

| Addressing Modes                      | Syntax                  |
|---------------------------------------|-------------------------|
| Register Indirect Addressing          |                         |
| Register Indirect                     | (An)                    |
| Postincrement Register Indirect       | (An) +                  |
| Predecrement Register Indirect        | - (An)                  |
| Register Indirect with Offset         | d <sub>16</sub> (An)    |
| Indexed Register Indirect with Offset | d <sub>8</sub> (An, Xn) |
| Immediate Data Addressing             |                         |
| Immediate                             | = XXX                   |
| Quick Immediate                       | = 1 - = 8               |
| Implied Addressing                    |                         |
| Implied Register                      | SR/USP/SP/PC            |

Notes:

Dn = Data Register

An = Address Register

Xn = Address of Data Register used as Index Register

SR = Status Register

PC = Program Counter

SP = Stack Pointer

USP = User Stack Pointer

( ) = Effective Address

d<sub>8</sub> = 8-bit Offset (Displacement)d<sub>16</sub> = 16-bit Offset (Displacement)

= xxx = Immediate Data

**Table 2-11.** Instruction Set Summary

| Mnemonic | Description                          |
|----------|--------------------------------------|
| ABCD     | Add Decimal with Extend              |
| ADD      | Add                                  |
| AND      | Logical AND                          |
| ASL      | Arithmetic Shift Left                |
| ASR      | Arithmetic Shift Right               |
| Bcc      | Branch Conditionally                 |
| BCHG     | Bit Test and Change                  |
| BCLR     | Bit Test and Clear                   |
| BRA      | Branch Always                        |
| BSET     | Bit Test and Set                     |
| BSR      | Branch to Subroutine                 |
| BTST     | Bit Test                             |
| CHK      | Check Register Against Bounds        |
| CLR      | Clear Operand                        |
| CMP      | Compare                              |
| DBcc     | Test Condition, Decrement and Branch |
| DIVS     | Signed Divide                        |
| DIVU     | Unsigned Divide                      |
| EOR      | Exclusive OR                         |
| EXG      | Exchange Registers                   |
| EXT      | Sign Extend                          |
| JMP      | Jump                                 |
| JSR      | Jump to Subroutine                   |
| LEA      | Load Effective Address               |
| LINK     | Link Stack                           |
| LSL      | Logical Shift Left                   |
| LSR      | Logical Shift Right                  |
| MOVE     | Move                                 |
| MULS     | Signed Multiply                      |
| MULU     | Unsigned Multiply                    |
| NBCD     | Negate Decimal with Extend           |
| NEG      | Negate                               |
| NOP      | No Operation                         |
| NOT      | One's Complement                     |
| OR       | Logical OR                           |
| PEA      | Push Effective Address               |

**Table 2-11.** Instruction Set Summary (Continued)

| Mnemonic | Description                  |
|----------|------------------------------|
| RESET    | Reset External Devices       |
| ROL      | Rotate Left without Extend   |
| ROR      | Rotate Right without Extend  |
| ROXL     | Rotate Left with Extend      |
| ROXR     | Rotate Right with Extend     |
| RTE      | Return from Exception        |
| RTR      | Return and Restore           |
| RTS      | Return from Subroutine       |
| SBCD     | Subtract Decimal with Extend |
| Scc      | Set Conditional              |
| STOP     | Stop                         |
| SUB      | Subtract                     |
| SWAP     | Swap Data Register Halves    |
| TAS      | Test and Set Operand         |
| TRAP     | Trap                         |
| TRAPV    | Trap on Overflow             |
| TST      | Test                         |
| UNLK     | Unlink                       |

### 2.7.3.3 Read Modify Write Cycle

The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the TS68C000, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This Instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write are byte operations.

### 2.7.4 Instruction Set Overview

The TS68C000 instruction set is shown in [Table 2-11](#). Some additional instructions are variations, or sub-sets, of these and they appear in [Table 2-12](#). Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps).

**Table 2-12.** Variations of Instruction Types

| Instruction Type | Variation                                                                                         | Description                                                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADD              | ADD<br>ADDA<br>ADDQ<br>ADDI<br>ADDX                                                               | Add<br>Add Address<br>Add Quick<br>Add Immediate<br>Add with Extend                                                                                                                                 |
| AND              | AND<br>ANDI<br>ANDI to CCR<br>ANDI to SR                                                          | Logical AND<br>And Immediate<br>And Immediate to Condition codes<br>And Immediate to Status Register                                                                                                |
| CMP              | CMP<br>CMPA<br>CMPM<br>CMPI                                                                       | Compare<br>Compare Address<br>Compare Memory<br>Compare Immediate                                                                                                                                   |
| EOR              | EOR<br>EORI<br>EORI to CCR<br>EORI to SR                                                          | Exclusive OR<br>Exclusive OR Immediate<br>Exclusive OR Immediate to condition Codes<br>Exclusive OR Immediate to Status Register                                                                    |
| MOVE             | MOVE<br>MOVEA<br>MOVEM<br>MOVEP<br>MOVEQ<br>MOVE from SR<br>MOVE to SR<br>MOVE to CCR<br>MOVE USP | Move<br>Move Address<br>Move Multiple Registers<br>Move Peripheral Data<br>Move Quick<br>Move from Status Register<br>Move to Status Register<br>Move to Condition Codes<br>Move User Stack Pointer |
| NEG              | NEG<br>NEGX                                                                                       | Negate<br>Negate with Extend                                                                                                                                                                        |
| OR               | OR<br>ORI<br>ORI to CCR<br>ORI to SR                                                              | Logical OR<br>OR Immediate<br>OR Immediate to Condition Codes<br>OR Immediate to Status Register                                                                                                    |
| SUB              | SUB<br>SUBA<br>SUBI<br>SUBQ<br>SUBX                                                               | Subtract<br>Subtract Address<br>Subtract Immediate<br>Subtract Quick<br>Subtract Extend                                                                                                             |

## 2.7.5 Processing States

The TS68C000 is always in one of three processing states: normal, exception, or halted.

### 2.7.5.1 Normal Processing

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

### 2.7.5.2 Exception Processing

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

### 2.7.5.3 Halted Processing

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

Asserting the reset and halt line for ten cycles will cause a processor reset, except when VCC is initially applied to the processor. In this case, an external reset must be applied for least 100 milliseconds.

## 2.7.6 Interface with EF 6800 Peripherals

Extensive line of EF6800 peripherals are directly compatible with the TS68C000.

Note: It is the own user's responsibility to verify the actual EF 6800 peripheral performances to be compatible to the actual used TS68C000 microprocessor performances.

Some of the EF 6800 peripheral that are particularly useful are:

EF6821: Peripheral Interface Adapter

EF6840: Programmable Timer Module

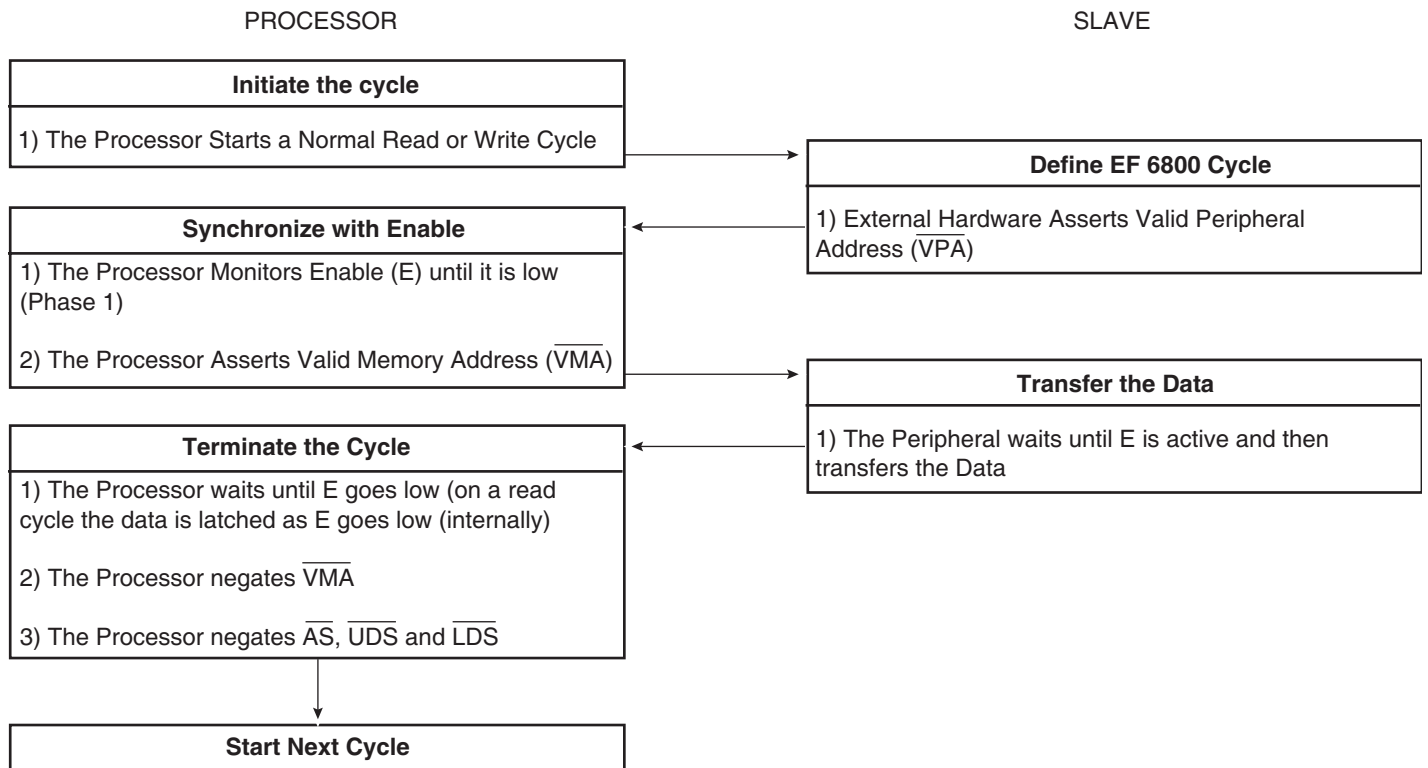
EF6850: Asynchronous Communications Interface Adapter

EF6852: Synchronous Serial Data Adapter

EF6854: Advanced Data Link Controller

To interface the synchronous EF 6800 peripherals with the asynchronous TS68C000, the processor modifies its bus cycle to meet the EF 6800 cycle requirements whenever an EF 6800 device address is detected. This is possible since both processors use memory mapped I/O. [Figure 2-13](#) is a flowchart of the interface operation between the processor and EF 6800 devices.

**Figure 2-13.** EF6800 Interfacing Flowchart



#### 2.7.6.1 Data Transfer Operation

Three signals on processor provide the EF 6800 interface. They are: enable (E), valid memory address ( $\overline{VMA}$ ), and valid peripheral address ( $\overline{VPA}$ ). Enable corresponds to the E or phase 2 signal in existing EF 6800 systems. The bus frequency is one tenth of the incoming TS68C000 clock frequency. The timing of E allows 1 MHz peripherals to be used 8 MHz TS68C000. Enable has a 60/40 duty cycle, that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive  $\overline{VPA}$  accesses on successive E pulses.

EF6800 cycle timing is given in [Figure 2-17](#) and [Figure 2-18](#). At state zero (50) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe ( $\overline{AS}$ ) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write ( $R/\overline{W}$ ) signal is switched to low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of  $\overline{VPA}$ .

The  $\overline{VPA}$  input signals the processor that the address on the bus is the address of an EF 6800 device (or an area reserved for EF6800 devices) and that the bus should conform to the phase 2 transfer characteristics of the EF 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the EF 6800 peripherals should be derived by decoding the address bus conditioned by  $\overline{VMA}$ .

After recognition of  $\overline{VPA}$ , the processor assures that the enable (E) is low, by waiting if necessary, and subsequently asserts  $\overline{VMA}$ . Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the EF6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the signal. Figure 2-17 and Figure 2-18 depict the best and worst case EF6800 cycle timing. This cycle length is dependent strictly upon when  $\overline{VPA}$  is asserted in relationship to the E clock.

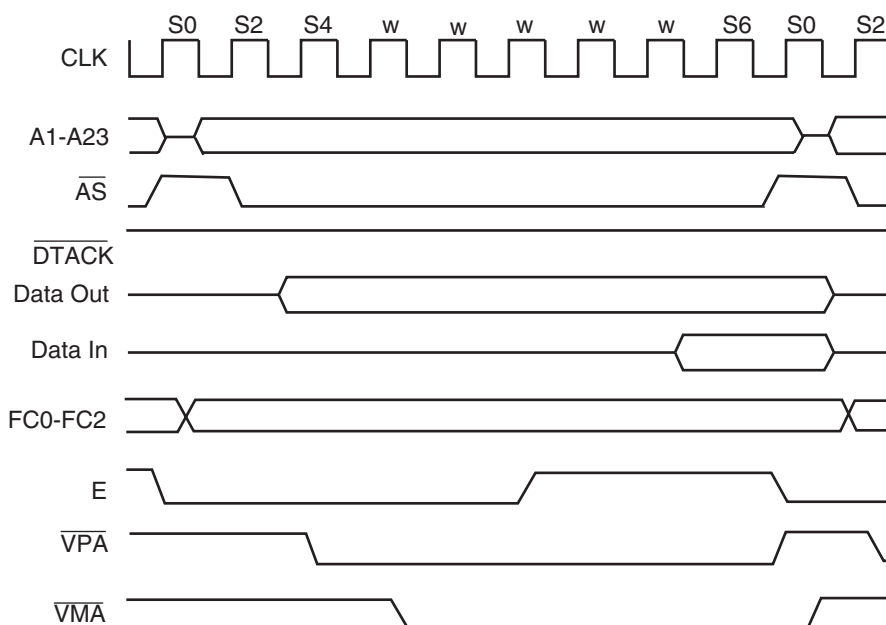
If it is assumed that external circuitry asserts  $\overline{VPA}$  as soon as possible after the assertion of  $\overline{AS}$ , then  $\overline{VPA}$  will be recognized as being asserted on the falling edge of 54. In this case, no "extra" wait cycles will be inserted prior to the recognition of  $\overline{VPA}$  asserted and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case –  $\overline{VPA}$  is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).
2. Worst Case –  $\overline{VPA}$  is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

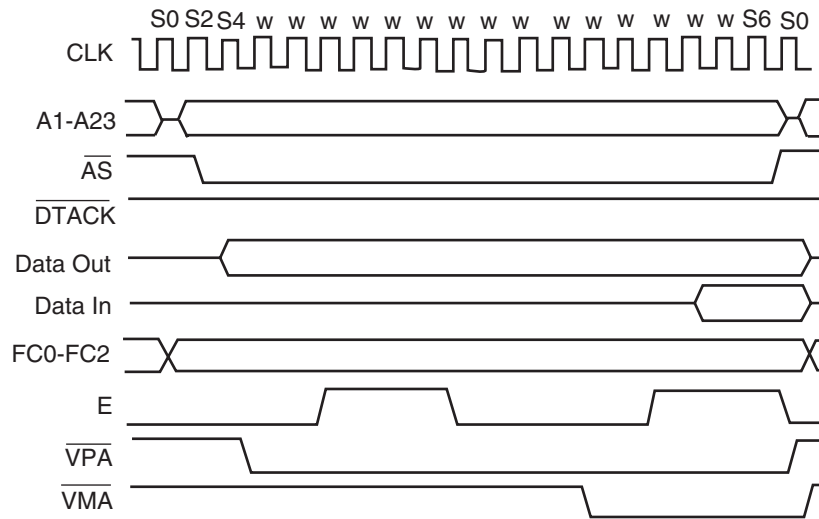
During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one-half clock cycle later in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove  $\overline{VPA}$  within one clock after the address strobe is negated.

$\overline{DTACK}$  should not be asserted while  $\overline{VPA}$  is asserted. Notice that the TS68C000  $\overline{VMA}$  is active low, contrasted with the active high EF 6800  $\overline{VMA}$ . This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting the peripherals.

**Figure 2-14.** TS68C000 to EF6800 Peripheral Timing – Best Case



**Figure 2-15.** TS68C000 to EF6800 Peripheral Timing – Worst Case



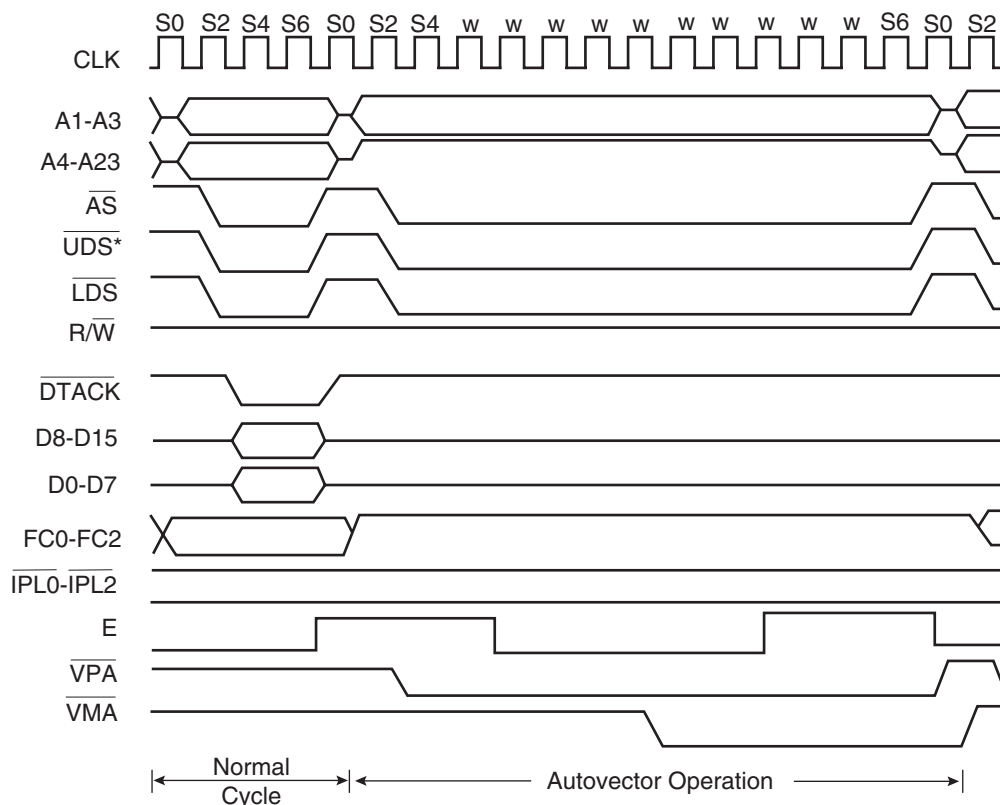
#### 2.7.6.2 Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the  $\overline{VPA}$  is asserted, the TS68C000 will assert  $\overline{VMA}$  and complete a normal EF 6800 read cycle as shown in Figure 2-16. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the EF 6800 and the TS68C(XX)'s normal vectored interrupt, the Interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since  $\overline{VMA}$  is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.

**Figure 2-16.** Autovector Operation Timing Diagram



Although  $\overline{UDS}$  and  $\overline{LDS}$  are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally).

**Table 2-13.** Dynamic Electrical Characteristics TS68C000 to EF 6800 Peripheral

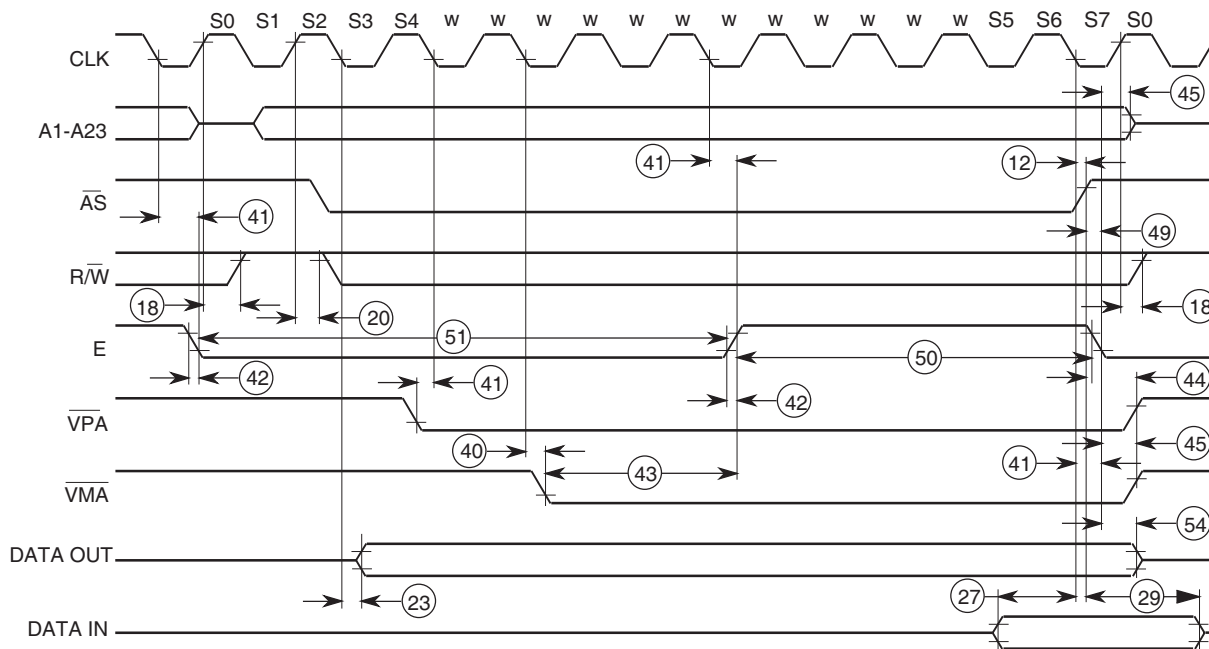
| Number | Symbol | Parameter                                                                     | 8 MHz  |     | 10 MHz |     | 12.5 MHz |     | Unit |
|--------|--------|-------------------------------------------------------------------------------|--------|-----|--------|-----|----------|-----|------|
|        |        |                                                                               | Limits |     | Limits |     | Limits   |     |      |
|        |        |                                                                               | Min    | Max | Min    | Max | Min      | Max |      |
| 12     | CLSH   | Clock low to $\overline{AS}$ , $\overline{DS}$ high <sup>(1)</sup>            |        | 70  |        | 55  |          | 50  | ns   |
| 18     | CHRH   | Clock high to $R/\overline{W}$ high <sup>(1)</sup>                            | 0      | 70  | 0      | 60  | 0        | 60  | ns   |
| 20     | CHRL   | Clock high to $R/\overline{W}$ low (write) <sup>(1)</sup>                     |        | 70  |        | 60  |          | 60  | ns   |
| 23     | CLDO   | Clock low to data out valid (write)                                           |        | 70  |        | 55  |          | 55  | ns   |
| 27     | CLDO   | Data in to clock low (set up time on read) <sup>(2)</sup>                     | 15     |     | 10     |     | 10       |     | ns   |
| 29     | SHDII  | $\overline{AS}$ , $\overline{DS}$ high to Data in invalid (hold time on read) | 0      |     | 0      |     | 0        |     | ns   |
| 40     | CLVML  | $\overline{AS}$ , $\overline{DS}$ high to $\overline{VPA}$ high               |        | 70  |        | 70  |          | 70  | ns   |
| 41     | CLET   | Clock low to E transition                                                     |        | 70  |        | 55  |          | 45  | ns   |
| 42     | Erf    | E output rise and fall time                                                   |        | 25  |        | 25  |          | 25  | ns   |
| 43     | VMLEH  | $\overline{VMA}$ low to E high                                                | 200    |     | 150    |     | 90       |     | ns   |
| 44     | SHVPH  | $\overline{AS}$ , $\overline{DS}$ high to $\overline{VPA}$ high               | 0      | 120 | 0      | 90  | 0        | 70  | ns   |

**Table 2-13.** Dynamic Electrical Characteristics TS68C000 to EF 6800 Peripheral (Continued)

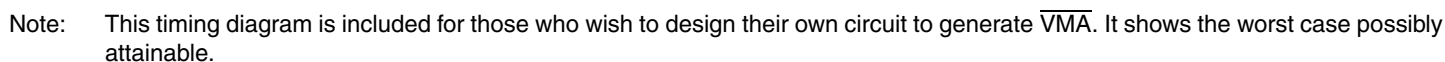
| Number | Symbol | Parameter                                                      | 8 MHz  |     | 10 MHz |     | 12.5 MHz |     | Unit |
|--------|--------|----------------------------------------------------------------|--------|-----|--------|-----|----------|-----|------|
|        |        |                                                                | Limits |     | Limits |     | Limits   |     |      |
|        |        |                                                                | Min    | Max | Min    | Max | Min      | Max |      |
| 45     | ELCAI  | E low to control, address bus invalid (address hold time)      | 30     |     | 10     |     | 10       |     | ns   |
| 47     | ASI    | Asynchronous input setup time <sup>(2)</sup>                   | 20     |     | 20     |     | 20       |     | ns   |
| 49     | SHEL   | $\overline{AS}$ , $\overline{DS}$ high to E low <sup>(3)</sup> | -70    | 70  | -55    | 55  | -80      |     | ns   |
| 50     | EH     | E width high                                                   | 450    |     | 350    |     | 280      |     | ns   |
| 51     | EL     | E width low                                                    | 700    |     | 550    |     | 440      |     | ns   |
| 54     | ELDOI  | E low to data out invalid                                      | 30     |     | 20     |     | 15       |     | ns   |

- Notes:
1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.
  2. If the asynchronous setup time (47) requirements are satisfied, the  $\overline{DTACK}$  low-to-data setup time (31) required can be ignored. The data must only satisfy the date in clock-low setup time (27) for the following cycle.
  3. The falling edge of S6 triggers both the negation of the strobes ( $\overline{AS}$  and  $\overline{XDS}$ ) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

**Figure 2-17.** TS68C000 to EF6800 Peripheral Timing Diagram – Best Case



Note: This timing diagram is included for those who wish to design their own circuit to generate  $\overline{VMA}$ . It shows the worst case possibly attainable.



Microcircuit are prepared for delivery in accordance with MIL-PRF-38535.

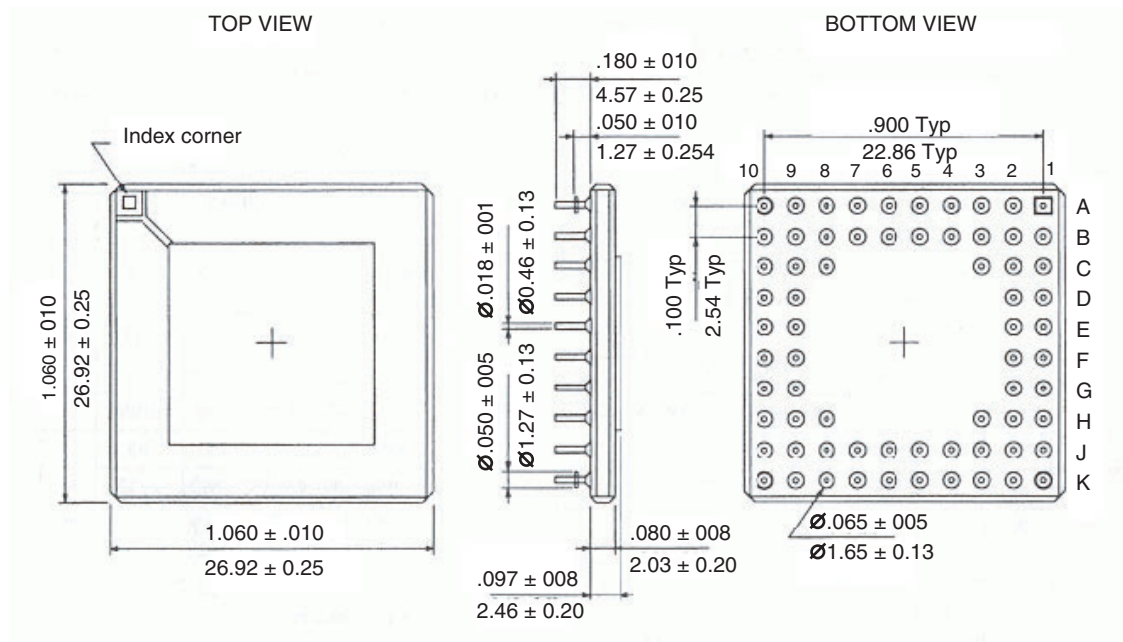
Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

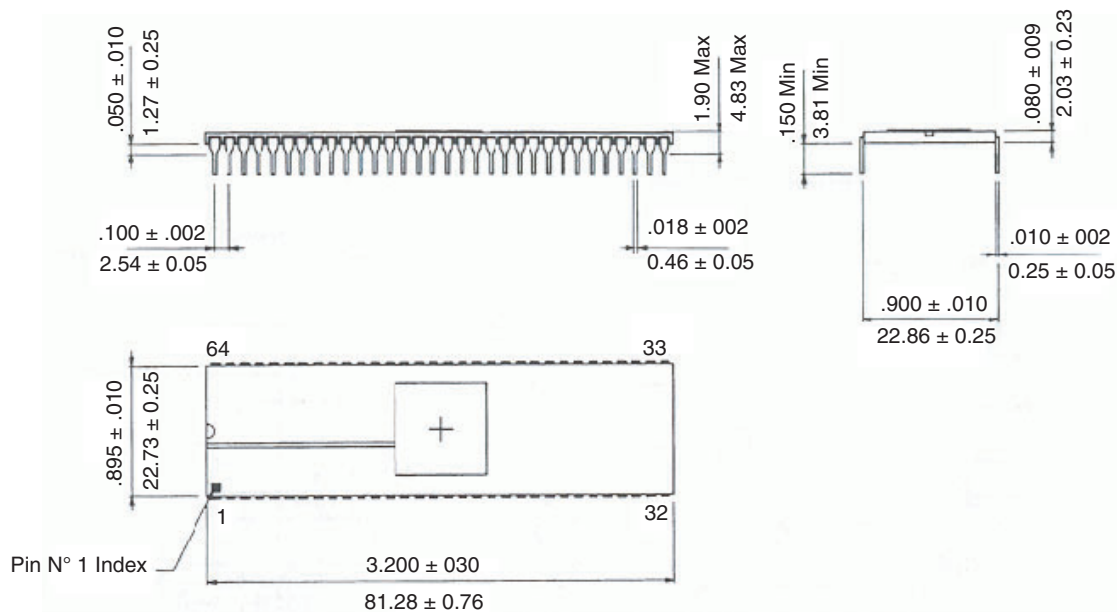
- a) Device should be handled on benches with conductive and grounded surface.
- b) Ground test equipment, tools and operator.
- c) Do not handle devices by the leads.
- d) Store devices in conductive foam or carriers.
- e) Avoid use of plastic, rubber, or silk in MOS areas.
- f) Maintain relative humidity above 50%, if practical.

## 2.10 Package Mechanical Data

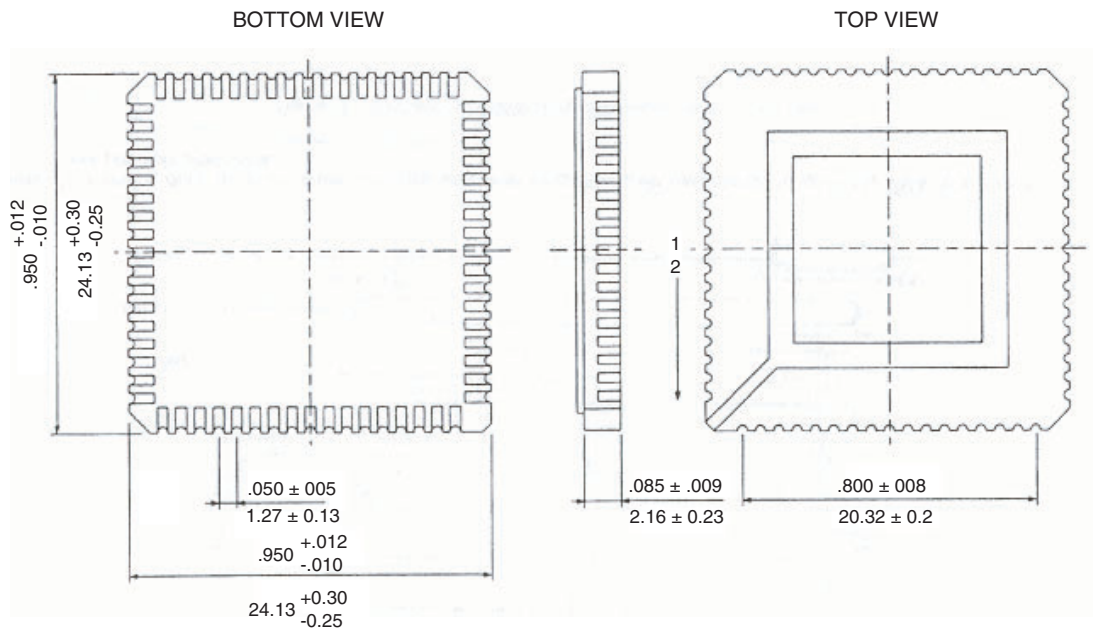
**Figure 2-19.** 68-lead – Pin Grid Array



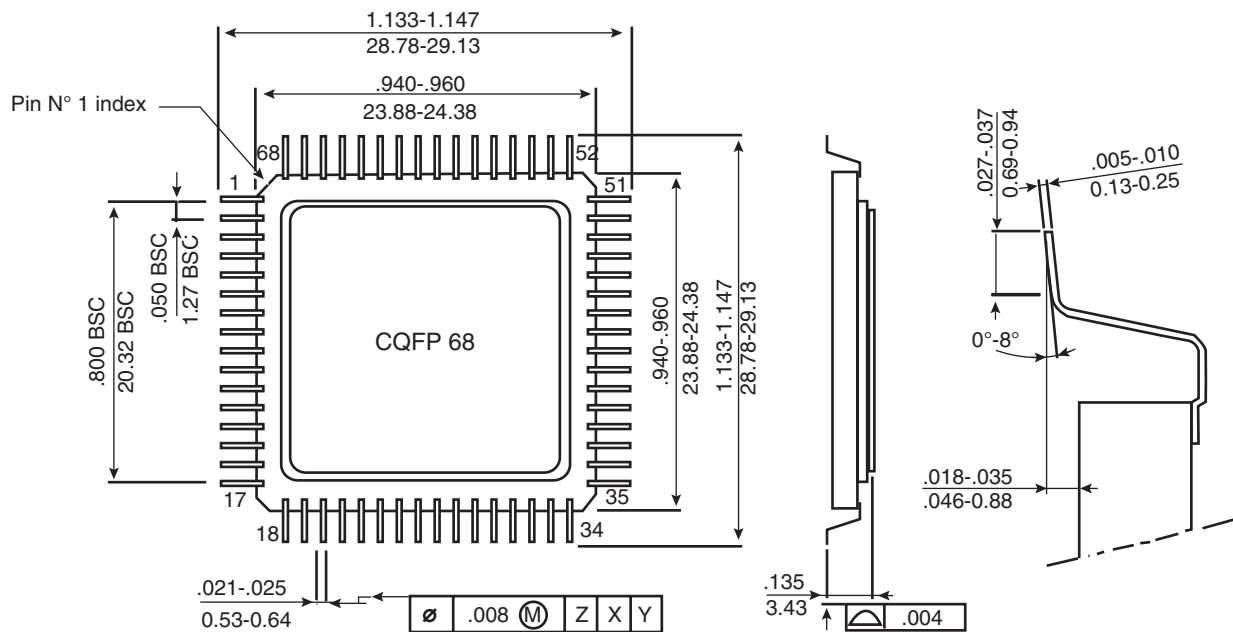
**Figure 2-20.** 64-lead – Ceramic Side Brazed Package



**Figure 2-21. 68-lead – Leadless Ceramic Chip Carrier**

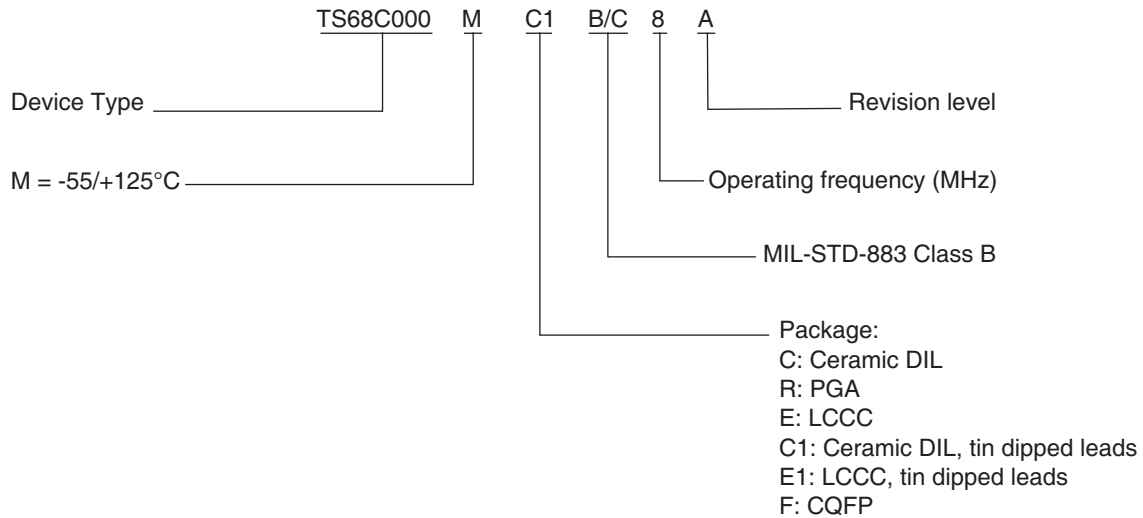


**Figure 2-22.** 68-lead – Ceramic Quad Flat Pack

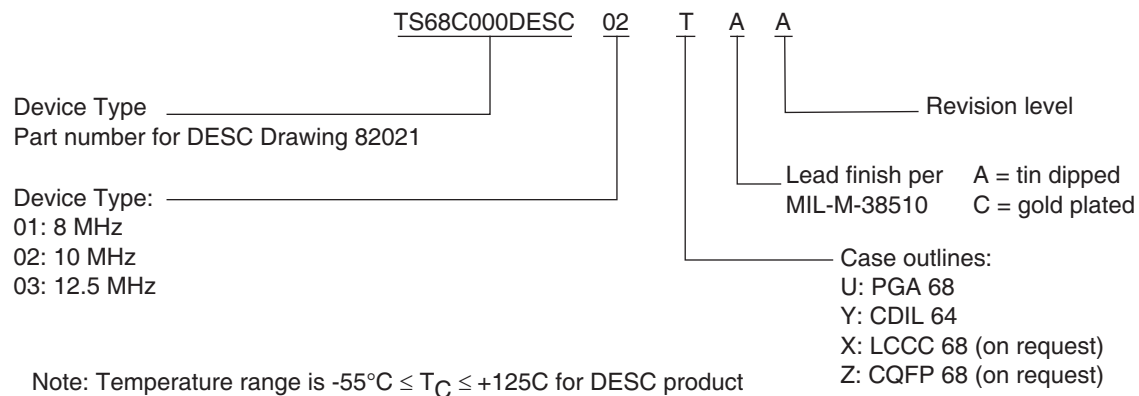


## 2.11 Ordering Information

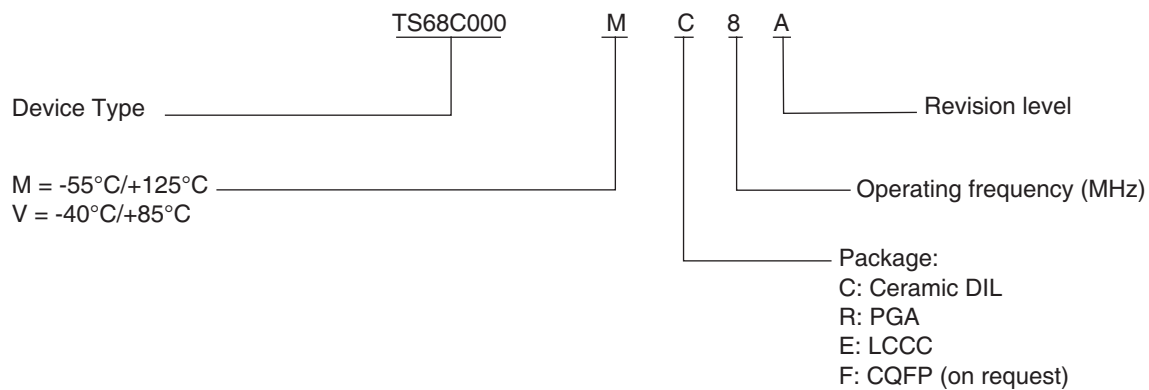
### 2.11.1 MIL-STD-883



### 2.11.2 DESC



## 2.11.3 Standard Product



Note: 1. For availability of the different versions, contact your Atmel sale office.



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